µCSP: A Diminutive, Hybrid, Space Processor for Smart Modules and CubeSats

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ABSTRACT

The nature of on-board, satellite computing systems is evolving, from centralized to distributed systems, so as to reap benefits in performance, scalability, configurability, and dependability. These distributed systems will feature space computers and smart modules (e.g., smart instruments, smart actuators), each with capability for networking and processing. To address processing and networking needs of future smart modules, as well as improve computing capability for lower-end CubeSats, we developed a new system known as µCSP. Like its more powerful counterpart, the CSPv1, µCSP is designed with a hybrid mix of commercial and radiation-hardened components supplemented with mechanisms from fault-tolerant computing. µCSP also features a hybrid processor architecture, with a mix of fixed and reconfigurable logic, but all in a smaller form factor with lower SWaP-C. µCSP is smaller than a credit card and designed to integrate into (but not be limited to) 1U SmallSat form factors. Research showcased in this paper also includes an overview of our concepts for smart modules in distributed computing systems for space, both within a single spacecraft and across multiple spacecraft, in terms of a framework for the construction of a variety of reusable, modular 1U boards with varying functionality for enhanced satellite capability and configuration.

I. INTRODUCTION

Spacecraft computing requirements for emerging and future missions are rapidly escalating, due to higher degrees of sophistication in remote sensing, autonomous control, and remote communications. Additionally, the committee on assessment of NASA's Earth science program found that the program's budget is inadequate in relation to its needs. This finding notes that NASA, confronted with these challenges, must strive even further to "do more with less" and plan missions with a fully cost-aware approach [1].

> *"… implement its missions via a cost-constrained approach, requiring that cost partially or fully constrain the scope of each mission such that realistic science and applications objectives can be accomplished within a reasonable and achievable future budget scenario"*

In this mindset for electronic design, industry and government organizations are striving to find next-generation processing systems that meet the constrained needs of future missions, namely low power, low cost, and high performance [2].

Space is a hazardous environment for electronic components, and systems that are deployed into this environment are plagued with failure modes and effects from the harsh environment. Radiation sources that cause concerns for spacecraft design include the Van Allen belts, magnetosphere, galactic cosmic rays, and solar weather [3]. There are both long- and short-term effects on electronics due to radiation. Temporal (short-term) effects, referred to as single-event effects (SEE), occur when a highly charged particle strikes a device. These events can be destructive or nondestructive and result in a number of failure effects. Cumulative (long-term) effects are characterized by radiation doses acquired over time, which will eventually cause a device to go out of its specification [4].

The National Research Council's midterm assessment of NASA's implementation of the Decadal Survey found that the nation's Earth observing system was beginning a decline in capability as older satellites are decommissioned. The assessment also found that new satellites have been plagued by budget cuts, launch failures, and other delays. To address these issues, it was recommended that NASA's Earth Science division should design around more stringent cost constraints and re-scope science objectives to accomplish missions within a lower cost bracket for a more achievable future budget. It was also suggested in the survey that alternative platforms and flight formations could be

employed as low-cost solutions for meeting science objectives and maturing remote sensing technologies. The Earth science budget varies, depending upon congress for each fiscal year, therefore a new framework for Earth observation is needed to be more resistant to funding fluctuations.

> *"… a number of promising alternative platforms and observing strategies are emerging and being proven. These include … small satellites … and the flight of multiple sensors in formations"*

II. BACKGROUND

This section provides a cursory overview of the benefits, challenges, and concerns of CubeSat technology, which is the targeted technology area for the µCSP. Additionally, this section discusses the benefits of distributed computing in space and research proposals involving those concepts, which can be enabled with µCSP using smart modules.

CubeSat and SmallSat Computing

CubeSats are one disruptive innovation that could be a possible solution to NASA's space computing challenges. The standard CubeSat form factor, typically 10 cm^3 and < 1 kg, was pioneered by Bob Twiggs and Jordi Puig-Suari in 1999 [5]. Originally, these standardized small spacecraft were conceived for education and flight tests. However, since their conception, government and commercial sectors have envisioned a greater role for CubeSats [5]. CubeSats have been described as flexible platforms that can perform NASA-class science investigations and technology demonstrations at a fraction of the cost of traditional satellites. NASA Goddard's Chief Technologist of Applied Engineering Technology Directorate, Michael Johnson, described CubeSats as [6]:

> *"… a transformational technology that gives us a way to dramatically change the way we do science"*

In addition to their low-cost development, CubeSats enable new mission configurations by deploying a swarm or constellation of the platforms [6]. There are many benefits for missions featuring a swarm of CubeSats. Depending upon the desired level of redundancy, CubeSat swarms can suffer the loss of several spacecraft, by distributing the work across the swarm, while failed spacecraft are quickly replaced due to their high reproducibility. Finally, multiple satellites can also provide scientists with a scientific advantage by providing multiple data points. One key demonstration of this capability comes from Planet Labs, successfully launching a constellation of CubeSats to image the Earth [5].

At first inspection, CubeSats seem to be comprehensive solution, but they are not without their downsides. As indicated by [6] and [7], depending upon how they are analyzed, CubeSats can have an immensely high failure rate. This failure rate is less representative of the technology and more reflective of the range in experience of CubeSat designers. Generally, these reports represent a large spectrum of skillset levels, from simple university projects to fully supported NASA missions. Finally, due to the small form-factor and low-power budgets, CubeSats cannot power many of NASA's more formidable scientific instruments, and there are limits to the technology that can be miniaturized for SmallSat missions. Lastly, some instruments simply cannot be supported due to the physical payload volume [6] [8].

Distributed Space Computing and CubeSat Swarms

The concept of using multiple spacecraft for a single mission is not novel. CubeSats benefit from being able to distribute functions, such that the loss of one or two units is not catastrophic, since the remaining swarm members can compensate until a replacement is launched [8]. Two original descriptors for distributed space computing are fractionated spacecraft and disaggregated spacecraft. Fractionated spacecraft is a term first described in [9], by Brown and Eremenko at DARPA. In this concept, a traditional monolithic spacecraft would be replaced with distributed networks of small fractionated spacecraft working together in a cluster, to provide the same overall capability as a large satellite at reduced cost. This revolutionary concept was best represented by the System F6 program at DARPA, which sought to prove these concepts with a flight demonstration [10]. The US Air Force Space Command also recognized the need for this concept and released a white paper [11] proposing a nearly identical concept for disaggregated space architectures emphasizing the benefit of redundancy to increase the difficulty of disabling operational capability by increasing the number of potential targets.

Modular Integrated Stackable Layers (MISL)

A requisite process, coinciding with the need for distributed computing, is the ability to rapidly create small spacecraft with the necessary capabilities for distributed functions. NASA Johnson's Controls and Data Handling Branch partnered with Texas A&M to develop a rapid prototyping architecture for hardware designs. Each design is defined as a "layer" that can be stacked together to quickly configure a testbed system for a variety of application domains. Each layer is designed separately and conforms to the NASA-managed MISL bus architecture guaranteeing interface compatibility for integration [12].

III. APPROACH

Due to the continued advances of CubeSat technology, there is a growing number of missions featuring off-the-shelf CubeSat kits supplied by commercial vendors. These kits frequently feature commercial components that have no previous flight heritage or radiation-testing results. As illustrated in [13], these kits typically include popular microcontrollers. However, these microcontrollers can fail due to the effects of radiation and also lack the processing capability to support more complex sensors. For CubeSats to be proven as a capable technology, CubeSat processing will have to improve. There is also a distinct need in the CubeSat community for a low-power yet capable platform that can rapidly be reconfigured for different missions as the number of SmallSat missions continues to increase [14]. This increasing trend for SmallSat missions is featured in Figure 1. Figure 1 illustrates past launches of CubeSats, with launch predictions for future years, displaying the full market potential (estimation based on publically announced launch intentions and market research) and the SpaceWorks forecast.

This paper proposes a novel system for space computing in terms of two distinct purposes:

(1) Enable a "smart module" framework for fast configuration and development of CubeSats by reducing design costs through design reuse.

(2) Provide a hybrid computer designed for high performance and dependability on highly power-constrained platforms.

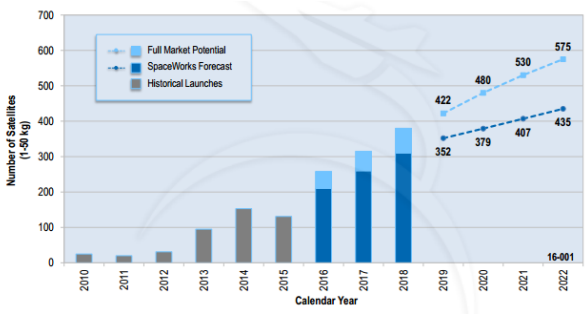

Figure 1: SpaceWork's Nano/Microsatellite Launch History and Forecast [14]

CSP: The Concept

µCSP follows the design concepts of the CHREC Space Processor (CSP) pioneered in CHREC at the University of Florida, in terms of hybrid and reconfigurable space computing. It features a multifaceted approach motivated, introduced, and detailed (in terms of CSPv1 implementation) in [15], [16], and [17]. In summary, the CSP concept focuses upon hybrid system and processor architectures. In CSP systems, commercial technology is featured for the best in high performance with low size, weight, power, and cost. For high dependability, radiation-hardened devices are also featured, monitoring and managing the commercial devices, which are further augmented with fault-tolerant computing. A hybrid processor is employed, which allows designers to optimize algorithms in terms of both fixed and reconfigurable logic in a System on Chip (SoC). The basic concept is illustrated in Figure 2.

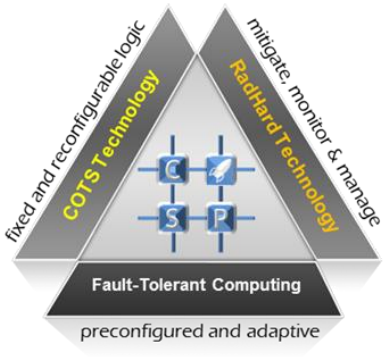

Figure 2: CSP Concept

Smart Modules: The Concept

Despite CubeSats having a common mechanical structure, the internal hardware design may drastically differ between implementations. Many CubeSats that are created are one-off designs, specific to each mission and its requirements. While these designs are different, there are design commonalities that must be present to guarantee functionality (e.g., power, communications). µCSP enables the concept of "smart modules" to address these design challenges.

The Smart Module concept has three main objectives:

(1) Provide "smart" capability to each design slice
(2) Achieve faster configuration and prototyping
(3) Exploit reuse of designs through qualification

The smart-module system is a framework for designing a series of hardware platforms that can be easily configured, integrated, and tested in preparation for a new mission. The main idea is to construct a series of hardware "cards" or "slices" that have the desired sensors and functionality while following the provided design template. Once the key sensors are identified, they are placed and routed into a hardware card. This hardware card is designed using a baseline template that features two high-density connectors, in the center of the board, a backplane connector, and (optionally) two network (e.g., SpaceWire) connectors (that can also be routed through the backplane). An example template is illustrated in Figure 3. The smart-module framework also enables configurable distributed systems.

Distributed configurations and processing can apply within a single spacecraft, with space computers (e.g., CSPs) and smart modules (e.g., instruments and actuators equipped with µCSPs). Wireless smart modules could also be developed to promote networking and distributed systems across spacecraft.

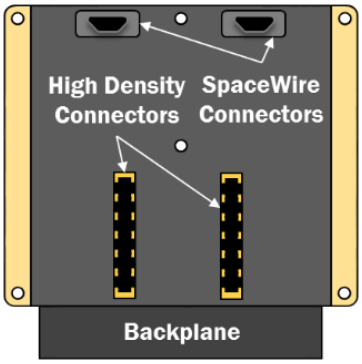

Figure 3: Example Template for Smart Module

The two high-density connectors shown are used to attach our new low-power, hybrid computer, µCSP, to the module. The card can also plug into a backplane board with the backplane connector. This backplane connector provides power, ground, and bus communications to each of the modules. A board connection and mating diagram is displayed in Figure 4. Finally, the two SpaceWire connectors link each module to the board above and below it, forming a ring network as seen in Figure 5.

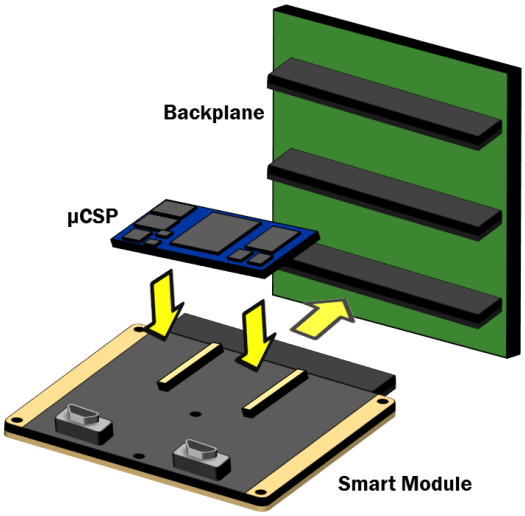

Figure 4: Integration and Mating with a Smart Module

The µCSP present on each card provides a smart module with low-power processing. µCSP can scale its power based upon the processing required for the node. One major benefit from this design is that once a hardware card is developed, it can be placed anywhere in the stack, due to the configurability of the connections. Once drivers and software are developed for the card, the card is portable and can be reused to rapidly prototype or assemble entire flight designs.

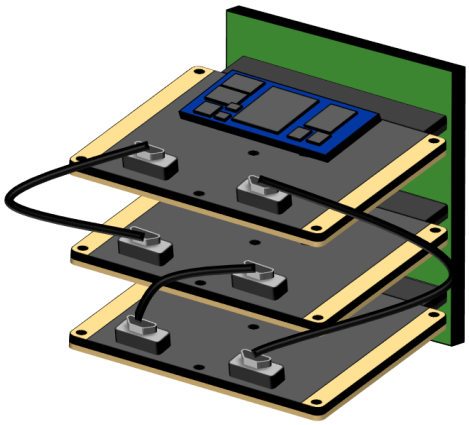

Figure 5: Ring Network Connection for Smart Module

Example devices are elaborated in [18] with examples summarized in Table 1 (e.g. Smart Thruster card).

Table 1: Examples of Smart Modules

Subsystem	Example Components
Power	Solar Cells Batteries Power Generator
Propulsion	Thruster Solar Sail
Communication	Transmitters Flight Terminal
Instruments	Optical Spectrometer Photometer Particle Detector
Attitude Determination and Control	Reaction Wheels Magnetorquer Control Moment Gyros Star Track Sun Sensors GPS Receiver and Antennas

As the "brain" for each smart module, µCSP allows designers to focus on their application and not on low-level implementation. After more of these hardware cards are developed, an inventory of designs is enabled that can be taken straight from "shelf-to-spacecraft."

IV. HARDWARE ARCHITECTURE

µCSP is designed to attach to a 1U CubeSat form-factor board (Smart Module), through two high-density connectors on the bottom. µCSP is roughly the size of a credit card (1.5" x 2.8") and 63 mils thick. An illustration of the top-down view of this board is

provided in Figure 6. All components for the board were purchased for an industrial temperature grade to support a temperature ranging from –40°C to +85°C.

µCSP can operate at 50 to 100 mW in a low-power standby mode and can be awakened with an interrupt. The nominal operational mode is estimated at 500 to 800 mW. Finally, we estimate maximum power with full utilization of the ARM Microcontroller Subsystem (MSS) and FPGA fabric at around 1 Watt.

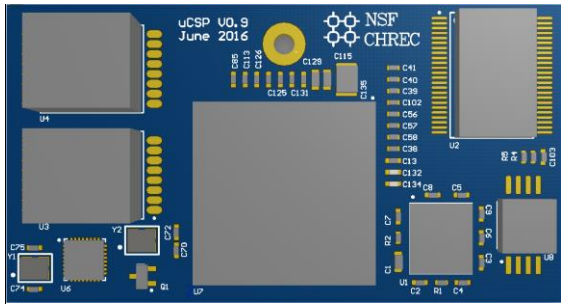

Figure 6: µCSP Computer Board

This new, small space computer has several main communication interfaces and I/O pins available. µCSP provides over 40 differential pairs (that can also be configured for single-ended operation). The board features two interfaces each for UART, I^2C, and SPI (4 slave-selects each). With the PHYs placed on the Smart Module, the µCSP can support one CAN and one USB2.0 interface. Our board has an Ethernet PHY to support 100 Mb/s connections, as well as 1 lane of PCI-Express. Finally, a JTAG interface is included to program and configure the device.

The inexpensive, commercial Emcraft SmartFustion2 System-on-Module (SoM) development platform can be fully interfaced with any designs following the Smart Module template. This approach allows Smart Module designs to be tested without a µCSP, solely using the Emcraft SoM, providing a cost-effective means of creating a ground-system testbed and performing verification. µCSP exhibits near complete pin compatibility with the SoM's evaluation board, albeit with some minor modifications. Finally, there are future plans for "carrier cards" with commercial components, which can be placed into the radiation-hardened footprints to assemble a commercial µCSP.

Device Selection

Adhering to the CSP concept, µCSP includes both commercial and radiation-hardened subsystems. Commercial components are featured for performance with low SWaP-C, and are closely managed by radiation-hardened or -tolerant components. Table 2 shows the key subsystem components in µCSP.

Table 2: Major Components of µCSP

Device	Vendor	Commercial / Radiation Hardened/Tolerant
Switching Regulators	3D-Plus	Radiation-Hardened
NOR Flash	Aeroflex	Radiation-Tolerant
Watchdog Timer	Intersil	Radiation-Hardened
SmartFusion2	Microsemi	Commercial
LPDDR	Intelligent Memory	Commercial

Processor Architecture

Microsemi's SmartFusion2 is a powerful, hybrid device featuring an ARM Cortex-M3 processor combined with a flash-based FPGA fabric. µCSP employs the m2s090 model, which is the most capable of the SmartFusion2 devices in a 484-pin package. Some key characteristics of the selected device are listed in Table 3.

Table 3: SmartFusion2 Specifications

ARM Specifications	
Maximum Clock Frequency	166 MHz
Instruction Cache	8 KB
Embedded SRAM (eSRAM)	64 KB
Embedded Nonvolatile Memory (eNVM)	512 KB
FPGA Specification	
Logic Elements	86,184
Math Blocks	84
SRAM Blocks	2074

V. SOFTWARE ARCHITECTURE

The featured technology on µCSP, the SmartFusion2 SoC, includes the ARM MSS (Cortex-M3) as its built-in hardcore processor. The Cortex-M3 was specifically developed to provide high performance at low power for microcontroller-type apps. This flexible platform can easily support two popular operating systems. The first supported is uClinux, which is an embedded Linux/Microcontroller project that ports Linux to systems that do not have a Memory Management Unit (MMU). U-boot can be installed on the on-chip, non-volatile memory to load uClinux and the root filesystem [19]. For apps that require determinism in execution, the Real-Time Operating System (RTOS) known as FreeRTOS can be booted to the Cortex-M3 [20].

Future work for µCSP involves integrating NASA Goddard's open-source, flight-system software, Core Flight Executive (cFE), and key supporting libraries and applications found in their Core Flight System

(cFS) to the SmartFusion2 in uClinux. Depending on availability and progress, cFS developers have a project in progress called micro-cFE to develop a minimal cFS flight-software framework specifically targeting small payloads and CubeSats that could be used in µCSP's build system [21].

VI. FAULT-TOLERANT ARCHITECTURE

µCSP includes fault-tolerance methods beyond its radiation-hardened and -tolerant components. The FPGA fabric of the SmartFusion2 is flash-based, which significantly differs from SRAM-based counterparts. While SRAM-based FPGAs are frequently affected by SEEs, the reconfigurable flash cell is resilient against SEEs [22], which makes flash-based FPGAs particularly useful for space-based apps.

µCSP includes a built-in hardware watchdog timer in the SmartFusion2, in addition to the external, hardened watchdog device by Intersil. This external watchdog is critically important to ameliorate radiation concerns for the operation of the SmartFusion2 in space. A whitepaper by Microsemi [23] states:

> *"… tests indicate that the IGLOO2 FPGAs and SmartFusion2 FPGAs encounter non-destructive latch-ups in heavy ion radiation testing, at energy levels low enough to cause concern in low earth orbit (LEO) space applications"*

This interim report was published in 2014, but was further investigated with additional testing in [24]. In [24], Single-Event Functional Interrupt (SEFI) behavior was more closely studied and four different recovery mechanisms were studied to recover the MSS if a SEFI occurred. These mechanisms included: (1) the MSS recovers by itself through time-out; (2) the MSS built-in watchdog recovers; (3) reset is issued to recover the MSS; (4) a full power cycle needed to recover. A full power cycle is required for certain components of the MSS for recovery, and consequently the Intersil hardware watchdog on µCSP will perform this reset function when triggered by lack of heartbeat from the SmartFusion2. Since watchdog reset of the system may be required under certain upset conditions, µCSP is only recommended for missions and flight applications where 100% availability is not a driving requirement.

SmartFusion2 also has several built-in reliability functions covered in [25]. Single Error Correct Double Error Detect (SECDED) protection can be turned on for several resources including Ethernet buffers, CAN message buffers, eSRAM, USB buffers, PCIe buffers, and DDR memory controllers. There are also buffers with SEU-resistant latches including DDR bridges, instruction cache, MMUART FIFOs, and SPI FIFOs. SmartFusion2 also has a built-in, self-test (BIST) mechanism that can be used to check status of the device automatically upon power-up or on demand. The BIST checks the contents of nonvolatile configuration memory, security keys, settings, and ROM memory pages. Lastly, there is no external configuration memory required to program and configure the device because it retains its configuration during a power cycle. The flash fabric is resistant to power "drop outs" during configuration, which would cause reliability issues for traditional SRAM-based FPGAs.

VII. SMART MODULES

In addition to the design of µCSP, several smart modules are in various stages of development and planning to showcase the versatility of µCSP, act as initial examples of types of smart modules to be created, and demonstrate a proof-of-concept, distributed space system. A CubeSat can be rapidly constructed once a library of validated designs has been generated for different smart module cards. This framework will significantly improve assembly and preparation for CubeSat missions and allow nearly identical spacecraft to be rapidly created. This system will allow configuration of a computing swarm with functionality distributed across multiple CubeSats. The framework will also allow fast construction of replacement spacecraft in the event of failures. The following is a list of smart-module designs now in development:

General Instrument Interface: This card is designed to interface with scientific instruments. It features ADCs, DACs, an RTC, and high-performance instrumentation amplifiers, as displayed in Figure 7.

BLDC Driver and Torque: This card is designed to potentially support an attitude control unit. It features three motor drivers, H-bridges, accelerometer, and gyroscope.

CMV4000 Image Sensor: This card features a 4.2-megapixel, 1" visual spectrum sensor. Additionally, the CMV4000 beneficially has a pin-compatible NIR variant, which can be used for more complex science experiments requiring different frequency bands.

Network-Attached Storage (NAS): This card is designed to support missions needing long-term data storage, or feature data sets that must be retained on-board because they cannot be downloaded quickly due to limited downlink bandwidth. This card will incorporate a fast memory for buffering from high-performance sensors, in addition to a large capacity of non-volatile (flash) memory for long-term storage.

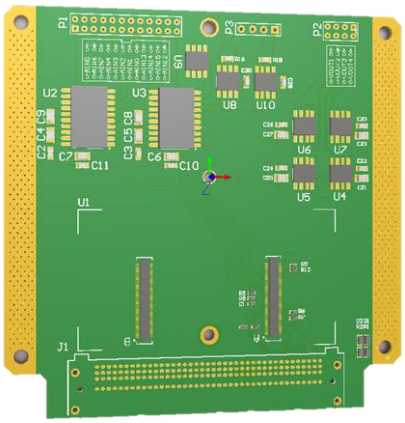

Figure 7: General Instrument Interface

Figure 8: Example of 6U CubeSat Wiring Harness

Another benefit of adhering to the Smart Module concept is reduction of extensive wiring that is found in some spacecraft. Figure 8 illustrates an example of required wiring for a 6U CubeSat. Smart modules place the processing intelligence closer to the sensor and actuators and employ a unified communications system, therefore reducing the bulk of the wiring for power and common communication interfaces. The reduction of wiring has a multitude of benefits:

(1) Reduces weight of spacecraft, thereby reducing cost by extension.

(2) Decreases integration and test time involved with building, assembling, and testing the wiring harness.

(3) Simplifies debugging and emulation of a system; since each subsystem will be composed of the same uCSP, there will be more design reuse and engineers will no longer have to be familiar with multiple interface standards.

VIII. CONCLUSIONS

There is a clear need for a high-performance computer for future CubeSat missions that are limited by highly limited power systems. µCSP is a small, low-cost, and low-power space computer designed to provide increased capability for SmallSat missions that need higher performance and reliability despite severe resources constraints in size, weight, power, and cost. Additionally, µCSP enables the realization of Smart Module in distributed space systems, which can provide fast configuration of spacecraft for missions, improve productivity, and reduce mission-specific redesign.

µCSP follows our original CSP Concept and features reconfigurable and multifaceted hybrid computing, with a hybrid-system and a hybrid-processing architecture in a small form factor. The µCSP hardware design, combined with a variety of fault-tolerant computing techniques, running flight-system software, provides users with an optimal combination of performance, energy efficiency, and reliability to satisfy a variety of space missions. Fast assembly and replication of CubeSats is a key milestone in creating a distributed-computing cluster for space, with functions distributed across different CubeSats, as well as developing replacements for failed modules in the swarm.

Acknowledgments

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References

1. Anthes, R. A. et al., “Earth Science and Applications from Space: A Midterm Assessment of NASA’s Implementation of the Decadal Survey,” Washington, DC: Space Studies Board, National Research Council, 2007.

2. Doyle. R., “Next Generation Flight Computing: A Joint Investment of NASA and AFRL,” Workshop on Spacecraft Flight Software, Pasadena, CA, Dec 12, 2013.

3. Sayil, S., “Space Radiation Effects on Technology and Human Biology and Proper Mitigation Techniques”, Texas Space Grant Consortium (TSGC) Higher Education Grant Final Report, July 2010.

4. Maurer, R., Fraeman, M., Martin, M., and D. Roth, "Harsh Environments: Space Radiation Environment, Effects, and Mitigation," Johns Hopkins APL Technical Digest, vol. 28, no. 1, pp. 17-29, 2008.

5. Gustafson, C. and S. Janson, "Think Big, Fly Small," Aerospace CrossLink Magazine, September 1, 2014.
6. Keesey, L., "Outer Space on a Budget," Featured Technologies, NASA Office of the Chief Technologist. Nov. 17, 2014. [Online]. Available: https://gsfctechnology.gsfc.nasa.gov/OuterBudge.html
7. Swartout, M., "CubeSat Mission Success (or Not): Trends and Recommendations," NASA Electronics Parts and Packaging Program (NEPP) 2015 Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center, Greenbelt, MD, June 23-26, 2015.
8. Gleber, M., "The Future of CubeSats," Aug. 15, 2014. [Online]. Available: http://www.nasa.gov/content/goddard/the-future-of-cubesats
9. Brown, O. and P. Eremenko, "The Value Proposition for Fractionated Space Architectures," AIAA Space 2006 Conf., San Jose, CA, September 19-21, 2006.
10. Foster. W., "DARPA Cancels Formation-flying Satellite Demo," SpaceNews, May 17, 2013. [Online]. Available: http://spacenews.com/35375darpa-cancels-formation-flying-satellite-demo/
11. *Resiliency and Disaggregated Space Architectures*. Air Force Space Command. [Online]. Available: http://www.ndiarmc.org/wp-content/uploads/2013/08/Resiliency-and-Disaggregated-Space-Architectures.pdf
12. Morgan, J. and J. Porter, "Modular Integrated Stackable Layer (MISL): An Academic-Public Sector Partnership for Rapid Prototyping and Development," 122nd ASEE Annu. Conf. & Expo. Seattle, WA, June 14-17, 2015.
13. Guertin. S., "CubeSat and Mobile Processors," NASA Electronics Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW) NASA Goddard Space Flight Center, Greenbelt, MD, June 23-26, 2015.
14. Doncaster, B. and J. Shulman, "2016 Nano/Microsatellite Market Forecast," SpaceWorks Enterprises, Inc. [Online]. Available: http://spaceworksforecast.com/2016-market-forecast/
15. George, A., "The Forthcoming Renaissance in Reconfigurable Space Computing," Proc. of Military and Aerospace Programmable Logic Devices Conf. (MAPLD), San Diego, CA, April 9-12, 2013.
16. Rudolph, D., Wilson, C., Stewart, J., Gauvin P., Crum, G., George, A., Wirthlin, M., Lam, H., "CSP: A Multifaceted Hybrid System for Space Computing," Proc. of 28th Annual AIAA/USU Conf. on Small Satellites, Logan, UT, August 2-7, 2014.
17. Wilson, C., Stewart, J., Gauvin, P., MacKinnon, J., Coole, J., Urriste, J., George, A., Crum, G., Wilson , A., Wirthlin, M., "CSP Hybrid Space Computing for STP-H5/ISEM on ISS," 29th Annual AIAA/USU Conf. on Small Satellites, Logan, UT, August 8-13, 2015.
18. Agasid, E. et al., "Small Spacecraft Technology State of the Art," NASA Ames Research Center, Mission Design Division, September, 2015.
19. *uClinux*. [Online]. Available: http://www.uclinux.org/
20. *SmartFusion2 RTOS, CLI and FAT Demo*. [Online]. Available: http://www.freertos.org/SmartFusion2_RTOS.html
21. *Core Flight Executive (cFE)*. [Online]. Available: http://opensource.gsfc.nasa.gov/projects/cfe/index.php
22. Wang, J., Rezzak, N., Dsilva, D., Huang, C. and K. Lee, "Single Event Effects Characterization in 65 nm Flash-Based FPGA-SOC," Single Event Effects (SEE) Symp. San Diego, CA, May 19th-22, 2014.
23. *IGLOO2 and SmartFusion2 65nm Commercial Flash FPGAs Interim Summary of Radiation Test Results*. Microsemi Corporation. October 21, 2014. [Online]. Available: http://www.microsemi.com/document-portal/doc_view/134103-igloo2-and-smartfusion2-fpgas-interim-radiation-report
24. Rezzak, N., Dsilva, D., Wang, J., and N. Jat, "SET and SEFI Characterization of the 65 nm SmartFusion2 Flash-Based FPGA under Heavy Ion Irradiation," Radiation Effects Data Workshop (REDW), 2015 IEEE, July 13-17, 2015.
25. *SmartFusion2 Reliability*. Microsemi Corporation. [Online]. Available: http://www.microsemi.com/products/fpga-soc/reliability/sf2-reliability