JOURNAL OF AEROSPACE INFORMATION SYSTEMS
Vol. 14, No. 3, March 2017

Comparative Analysis of Present and Future Space-Grade Processors with Device Metrics

Tyler M. Lovelly* and Alan D. George†
University of Florida, Gainesville, Florida 32611

DOI: 10.2514/1.I010472

Due to harsh and inaccessible operating environments, space computing presents many unique challenges and constraints that limit onboard computing performance. However, the increasing need for real-time sensor and autonomous processing, coupled with limited communication bandwidth with ground stations, is increasing onboard computing demands for next-generation space missions. Because currently available space-grade processors cannot satisfy this growing demand, research into various processors is conducted to ensure that potential new processors are based upon architectures that will best meet the computing needs of space missions. Device metrics are used to measure and compare the theoretical capabilities of processors based upon vendor-provided data and tools, enabling the study of large and diverse sets of architectures. Architectural tradeoffs are determined that can be considered when comparing or designing space-grade processors. Results demonstrate how onboard computing capabilities are increasing due to emerging architectures that support high levels of parallelism in terms of computational units, internal memories, and input/output resources; and that performance varies between applications, depending on the compute-intensive kernels used. Furthermore, the overheads incurred by radiation hardening are quantified and used to analyze low-power commercial-off-the-shelf processors for potential hardening and use in future space missions.

I. Introduction

MOST currently available space-grade processors are the result of commercial-off-the-shelf (COTS) processor architectures being selected for radiation hardening and use in space missions. Because creating space-grade processors is a lengthy, complex, and costly process, and because space mission design typically requires lengthy development cycles, there is a large and potentially growing technological gap between space-grade and COTS processors that results in limited and outdated processor options for space missions.

Although current space-grade processors increasingly lag behind the capabilities of emerging COTS processors [1–3], computing requirements for space missions are becoming more demanding due to the increasing need for real-time sensor and autonomous processing [4–6]. Furthermore, improving sensor technology and increasing mission data rates, data precisions, and problem sizes are increasing the demand for communication bandwidth to ground stations. Due to limited bandwidth and long transmission latencies, remote transmission of sensor data or real-time operating decisions become impractical for space missions. High-performance onboard computing can alleviate these challenges and address the unique computing needs of space missions by processing data before transmission to ground stations and making real-time operating decisions autonomously.

To address the continually increasing demand for high-performance onboard space computing, careful consideration is required when selecting processors for future space missions, and new architectures must be analyzed for potential new space-grade processors. Presently existing space-grade processors are typically based upon COTS processors with architectures that were not explicitly designed for the unique challenges of space computing. To ensure that new space-grade processors are based upon architectures that are most suitable for next-generation space missions, tradeoffs in architectural characteristics should be determined and considered when comparing or designing space-grade processors or when selecting a COTS architecture for hardening and use in space missions. However, the set of available processors is large and diverse, with many possible architectures to evaluate.

To analyze the large and diverse set of existing and potential future processor architectures for space computing, a suite of device metrics is leveraged that provides a theoretical basis for the study of architectural capabilities [7–10]. Facilitated by device metrics, quantitative analysis and objective comparisons are conducted for many diverse space-grade and low-power COTS processor architectures, from categories such as multicore and many-core central processing units (CPUs), digital signal processors (DSPs), field-programmable gate arrays (FPGAs), graphics processing units (GPUs), and hybrid configurations of these architectures. A device metrics analysis provides insights into the performance, power efficiency, memory bandwidth, and input/output bandwidth of specific implementations of these processors to track the current and future progress of their development and to determine which can best meet the computing needs of space missions. Although other metrics are also of interest, such as the cost and reliability of each processor, this information is not standardized between vendors and is often unavailable or highly dependent on mission-specific factors.

The remainder of this paper is structured as follows. Section II describes background and related research for space-grade processors and device metrics. Section III describes methodologies for the analysis of fixed-logic, reconfigurable-logic, and hybrid processors with device metrics. Section IV provides a comparative analysis of present and future space-grade processors with device metrics, including comparisons of space-grade processors to one another, in-depth analysis of how performance of space-grade processors varies between applications and kernels based on operations mix, comparisons of space-grade processors to the closest COTS counterparts upon which they were based to determine overheads incurred from hardening, and comparisons of top-performing space-grade and COTS processors to determine the potential for future space-grade processors. Finally, Sec. V provides conclusions and future research directions. Data for all results are tabulated and included in the Appendix.

Received 12 May 2016; revision received 14 January 2017; accepted for publication 19 January 2017; published online 6 March 2017.

*Ph.D. Candidate, NSF Center for High-Performance Reconfigurable Computing, Department of Electrical and Computer Engineering, 330 Benton Hall; lovelly@chrec.org.

†Professor, NSF Center for High-Performance Reconfigurable Computing, Department of Electrical and Computer Engineering, 327 Larsen Hall; george@chrec.org.

II. Background and Related Research

Many radiation hazards exist in the harsh space environment such as galactic cosmic rays, solar particle events, and trapped radiation in the Van Allen belts, which threaten the operation of onboard processors [11,12]. Space-grade processors must be radiation hardened or radiation tolerant to withstand cumulative radiation effects such as charge buildup within the gate oxide that causes damage to the silicon lattice over time, and they must provide immunity to single-event effects that occur when single particles pass through the silicon lattice and cause errors that can lead to data corruption or disrupt the functionality of the processor [13–15]. Several techniques exist for the fabrication of space-grade processors [16–18], including radiation hardening by process, which involves the use of an insulating oxide layer, and radiation hardening by design, which involves specialized transistor-layout techniques. Although both space-grade and COTS processors can be used in space, space-grade processors are often necessary, depending on the mission's orbit or location, planned lifetime, and requirements for reliability and accessibility. However, creating a space-grade version of a COTS processor often comes with associated costs [19], including slower operating frequencies, decreased numbers of processor cores or computational units, increased power dissipation, and decreased input/output resources. Traditionally, space-grade processors have come in the form of single-core CPUs [20]. However, in recent years, development has occurred on space-grade processors with more advanced architectures such as multicore and many-core CPUs, DSPs, and FPGAs.

To analyze and compare processors for use in space missions, an established set of device metrics is leveraged for the quantitative analysis of diverse processor architectures in terms of performance, power efficiency, memory bandwidth, and input/output bandwidth [7–10]. Device metrics provide a theoretical basis for the analysis of a processor's capabilities and enable the objective comparison of diverse architectures, from categories such as multicore and many-core CPUs, DSPs, FPGAs, GPUs, and hybrid configurations of these architectures. Device metrics can be calculated solely based upon architectural characteristics described by vendor-provided documentation and software tools, without the hardware costs and development efforts required for device benchmarking, thus providing a practical methodology for the comparison and analysis of a large and diverse set of processors. However, device metrics describe only the theoretical capabilities of each architecture without complete consideration of software requirements and implementation details, which may result in additional costs to performance, productivity, and other factors. Therefore, once the best processors have been identified with device metrics, more exhaustive hardware experimentation and analysis can then be conducted with device benchmarking to determine realizable capabilities.

Computational density (CD), reported in gigaoperations per second (GOPS), is a metric for the steady-state performance of a processor's computational units for a stream of independent operations. By default, calculations are based upon an operations mix of half-additions and half-multiplications. However, the default can be varied to analyze how performance differs between applications that contain kernels that require other operations mixes. Multiply–accumulate functions are only considered to be one operation each because they require data dependency between each addition and multiplication. CD is calculated separately for each data type considered, including 8 bit, 16 bit, and 32 bit integers, as well as both single-precision and double-precision floating points (hereafter referred to as Int8, Int16, Int32, SPFP, and DPFP, respectively). The CD per watt (CD/W), reported in GOPS per watt (GOPS/W), is a metric for the performance achieved for each watt of power dissipated by the processor. The internal memory bandwidth (IMB), reported in gigabytes per second, is a metric for the throughput between a processor and onchip memories. The external memory bandwidth (EMB), reported in gigabytes per second, is a metric for the throughput between a processor and offchip memories through dedicated memory controllers. The input/output bandwidth (IOB), reported in gigabytes per second, is a metric for the total throughput between a processor and offchip resources through both dedicated memory controllers and all other available forms of input/output. Although no single metric can completely characterize the performance of any given processor, each metric provides unique insight into specific architectural features that can be related to applications and kernels as needed. The most relevant metric for performance may be CD when bound computationally, CD/W when bound by power efficiency, IMB or EMB when bound by memory, IOB when bound by input/output resources, or some combination of multiple metrics depending on specific application requirements.

III. Device Metrics Methodology

To calculate device metrics for a fixed-logic processor such as a CPU, DSP, or GPU, several key pieces of information are required about the architecture that are obtained from vendor-provided documentation [7,8]. For example, Eqs. (1–15) demonstrate the process of calculating device metrics for Freescale QorIQ® P5040, which is a quadcore CPU [21–23]. CD calculations require information about the operating frequency, the number of each type of computational unit, and the number of operations per cycle that can be achieved by each type of computational unit for all operations mixes and data types considered. As shown in Eqs. (1) and (2), there is one-integer addition unit and one-integer multiplication unit on each processor core, allowing for one addition and one multiplication to be issued simultaneously per cycle for all integer data types. There is only one floating-point unit on each processor core, which handles both additions and multiplications, allowing for only one operation to be issued per cycle for all floating-point data types. CD/W calculations require the same information as CD calculations, in addition to the maximum power dissipation. As shown in Eqs. (3) and (4), the CD/W is calculated using the corresponding CD calculations and the maximum power dissipation. IMB calculations require information about the number of each type of onchip memory unit, such as caches and register files, and associated operating frequencies, bus widths, access latencies, and data rates. As shown in Eqs. (5–7), the IMB is calculated for all types of caches available on each processor core. Assuming cache hits, both types of L1 cache can supply data in each clock cycle. Although the L2 cache has a higher bus width, it also requires a substantial access latency, which limits the overall bandwidth. IMB values are combined to obtain the total IMB. EMB calculations require information about the number of each type of dedicated controller for offchip memories and associated operating frequencies, bus widths, and data rates. As shown in Eq. (8), the EMB is calculated for the dedicated controllers available for external memories on the QorIQ P5040. IOB calculations require the same information as EMB calculations, in addition to the number of each type of available input/output resource and associated operating frequencies, bus widths, and data rates. As shown in Eqs. (9–15), the IOB is calculated for each type of input/output resource available using optimal configurations for signal multiplexing. IOB values are combined to obtain the total IOB:

$$\mathrm{CD}_{\mathrm{Int8/Int16/Int32}} = 2.2\ \mathrm{GHz} \times 4\ \mathrm{cores} \times 2\ \mathrm{units} \times 1\ \mathrm{operation/cycle} = 17.60\ \mathrm{GOPS} \tag{1}$$

$$\mathrm{CD}_{\mathrm{SPFP/DPFP}} = 2.2\ \mathrm{GHz} \times 4\ \mathrm{cores} \times 1\ \mathrm{unit} \times 1\ \mathrm{operation/cycle} = 8.80\ \mathrm{GOPS} \tag{2}$$

$$\mathrm{CD/W}_{\mathrm{Int8/Int16/Int32}} = \mathrm{CD}_{\mathrm{Int8/Int16/Int32}}/49\ \mathrm{W} = 0.36\ \mathrm{GOPS/W} \tag{3}$$

$$\mathrm{CD/W}_{\mathrm{SPFP/DPFP}} = \mathrm{CD}_{\mathrm{SPFP/DPFP}}/49\ \mathrm{W} = 0.18\ \mathrm{GOPS/W} \tag{4}$$

$$\mathrm{IMB}_{\mathrm{L1\ data\ cache}} = 2.2\ \mathrm{GHz} \times 4\ \mathrm{cores} \times 8\ \mathrm{B\ bus} = 70.40\ \mathrm{GB/s} \tag{5}$$

$$\mathrm{IMB}_{\mathrm{L1\ instruction\ cache}} = 2.2\ \mathrm{GHz} \times 4\ \mathrm{cores} \times 16\ \mathrm{B\ bus} = 140.80\ \mathrm{GB/s} \tag{6}$$

$$\mathrm{IMB}_{\mathrm{L2\ cache}} = 2.2\ \mathrm{GHz} \times 4\ \mathrm{cores} \times 64\ \mathrm{B\ bus}/11\ \mathrm{cycle\ latency} = 51.20\ \mathrm{GB/s} \tag{7}$$

$$\mathrm{EMB}_{\mathrm{DDR3}} = 2\ \mathrm{controllers} \times 8\ \mathrm{B\ bus} \times 1600\ \mathrm{MT/s} = 25.60\ \mathrm{GB/s} \tag{8}$$

$$\mathrm{IOB}_{\mathrm{DDR3}} = \mathrm{EMB}_{\mathrm{DDR3}} = 25.60\ \mathrm{GB/s} \tag{9}$$

$$\mathrm{IOB}_{\mathrm{GPIO}} = 1.1\ \mathrm{GHz} \times 32\ \mathrm{ports} = 4.40\ \mathrm{GB/s} \tag{10}$$

$$\mathrm{IOB}_{\mathrm{PCIe2.0}} = 8\ \mathrm{lanes} \times 4\ \mathrm{Gb/s} \times 2\ \mathrm{full\ duplex} = 8.00\ \mathrm{GB/s} \tag{11}$$

$$\mathrm{IOB}_{\mathrm{10GigE}} = 8\ \mathrm{lanes} \times 2.5\ \mathrm{Gb/s} \times 2\ \mathrm{full\ duplex} = 5.00\ \mathrm{GB/s} \tag{12}$$

$$\mathrm{IOB}_{\mathrm{1GigE}} = 2\ \mathrm{lanes} \times 1\ \mathrm{Gb/s} \times 2\ \mathrm{full\ duplex} = 0.50\ \mathrm{GB/s} \tag{13}$$

$$\mathrm{IOB}_{\mathrm{SATA2.0}} = 2\ \mathrm{lanes} \times 2.4\ \mathrm{Gb/s} = 0.60\ \mathrm{GB/s} \tag{14}$$

$$\mathrm{IOB}_{\mathrm{SPI}} = 0.49\ \mathrm{Gb/s} \times 2\ \mathrm{full\ duplex} = 0.12\ \mathrm{GB/s} \tag{15}$$

To calculate device metrics for a reconfigurable-logic processor such as an FPGA, the process is more complex as compared to fixed-logic processors, and it requires several key pieces of information about the architecture that are obtained from vendor-provided documentation, software tools, and test cores [7–10]. For example, Eqs. (16–30) demonstrate the process of calculating device metrics for the Xilinx Virtex®-5 FX130T, which is an FPGA [24–27]. CD calculations require information about the total available logic resources of the architecture in terms of flip flops, lookup tables, and digital-signal-processing units. Additionally, the use of software tools and test cores is required to generate information about the operating frequencies and logic resources used for all operations mixes and data types considered [25,26]. A linear-programming algorithm is used for optimization, based upon operating frequencies and the configuration of computational units on the reconfigurable fabric [9,10]. As shown in Eqs. (16–20), the CD is calculated separately for each integer and floating-point data type, based upon the operating frequencies and logic resources used for additions and multiplications, where each computational unit can compute one operation per cycle and multiple versions of each computational unit are considered that make use of different types of logic resources. CD/W calculations require the use software tools to generate information about power dissipation given the configuration of computational units for each data type [27]. As shown in Eqs. (21–25), the CD/W is calculated separately for each integer and floating-point data type using estimates for maximum power dissipation generated with vendor-provided tools. IMB calculations require information about the number of onchip memory units such as block random-access-memory (BRAM) units and the associated operating frequencies, number of ports, bus widths, and data rates. As shown in Eq. (26), the IMB is calculated for the internal BRAM units on the Virtex-5. EMB calculations require the operating frequency, logic and input/output resource usage, bus widths, and data rates for dedicated controllers for offchip memories. As shown in Eq. (27), the EMB is calculated for dedicated controllers for external memories, where the maximum number of controllers is limited by the number of input/output ports available. IOB calculations require the same type of information that is required for fixed-logic processors. As shown in Eqs. (28–30), the IOB is calculated for each type of input/output resource available. IOB values are combined to obtain the total IOB:

$$\mathrm{CD}_{\mathrm{Int8}} = 353.35\ \mathrm{MHz} \times 2358\ \mathrm{cores} \times 1\ \mathrm{operation/cycle} = 833.20\ \mathrm{GOPS} \tag{16}$$

$$\mathrm{CD}_{\mathrm{Int16}} = 380.95\ \mathrm{MHz} \times 1092\ \mathrm{cores} \times 1\ \mathrm{operation/cycle} = 416.00\ \mathrm{GOPS} \tag{17}$$

$$\mathrm{CD}_{\mathrm{Int32}} = 301.93\ \mathrm{MHz} \times 298\ \mathrm{cores} \times 1\ \mathrm{operation/cycle} = 89.97\ \mathrm{GOPS} \tag{18}$$

$$\mathrm{CD}_{\mathrm{SPFP}} = 327.33\ \mathrm{MHz} \times 246\ \mathrm{cores} \times 1\ \mathrm{operation/cycle} = 80.52\ \mathrm{GOPS} \tag{19}$$

$$\mathrm{CD}_{\mathrm{DPFP}} = 161.39\ \mathrm{MHz} \times 108\ \mathrm{cores} \times 1\ \mathrm{operation/cycle} = 17.43\ \mathrm{GOPS} \tag{20}$$

$$\mathrm{CD/W}_{\mathrm{Int8}} = \mathrm{CD}_{\mathrm{Int8}}/15.87\ \mathrm{W} = 52.50\ \mathrm{GOPS/W} \tag{21}$$

$$\mathrm{CD/W}_{\mathrm{Int16}} = \mathrm{CD}_{\mathrm{Int16}}/16.83\ \mathrm{W} = 24.72\ \mathrm{GOPS/W} \tag{22}$$

$$\mathrm{CD/W}_{\mathrm{Int32}} = \mathrm{CD}_{\mathrm{Int32}}/14.07\ \mathrm{W} = 6.39\ \mathrm{GOPS/W} \tag{23}$$

$$\mathrm{CD/W_{SPFP}} = \mathrm{CD_{SPFP}}/13.28\ \mathrm{W} = 6.06\ \mathrm{GOPS/W} \tag{24}$$

$$\mathrm{CD/W_{DPFP}} = \mathrm{CD_{DPFP}}/8.00\ \mathrm{W} = 2.18\ \mathrm{GOPS/W} \tag{25}$$

$$\mathrm{IMB_{BRAM}} = 0.45\ \mathrm{GHz} \times 298\ \mathrm{units} \times 2\ \mathrm{ports} \times 9\ \mathrm{B\ bus} = 2413.80\ \mathrm{GB/s} \tag{26}$$

$$\mathrm{EMB_{DDR2}} = 0.26667\ \mathrm{GHz} \times 5\ \mathrm{controllers} \times 8\ \mathrm{B\ bus} \times 2\ \mathrm{double\ data} = 21.33\ \mathrm{GB/s} \tag{27}$$

$$\mathrm{IOB_{DDR2}} = \mathrm{EMB_{DDR2}} = 21.33\ \mathrm{GB/s} \tag{28}$$

$$\mathrm{IOB_{GTX}} = 20\ \mathrm{transceivers} \times 6.5\ \mathrm{Gb/s} = 16.25\ \mathrm{GB/s} \tag{29}$$

$$\mathrm{IOB_{GPIO}} = 840\ \mathrm{ports} \times 0.8\ \mathrm{Gb/s} = 84.00\ \mathrm{GB/s} \tag{30}$$

To calculate device metrics for a hybrid processor that contains some combination of CPU, DSP, GPU, and FPGA architectures, the calculations must first be completed for each constituent architecture. CD values are then combined to obtain the hybrid CD, which is then divided by the combined maximum power dissipation to obtain the hybrid CD/W. IMB, EMB, and IOB values are also combined to obtain the hybrid IMB, EMB, and IOB, but they must account for any overlap of memory and input/output resources that are shared between the constituent architectures.

IV. Experiments, Results, and Analysis

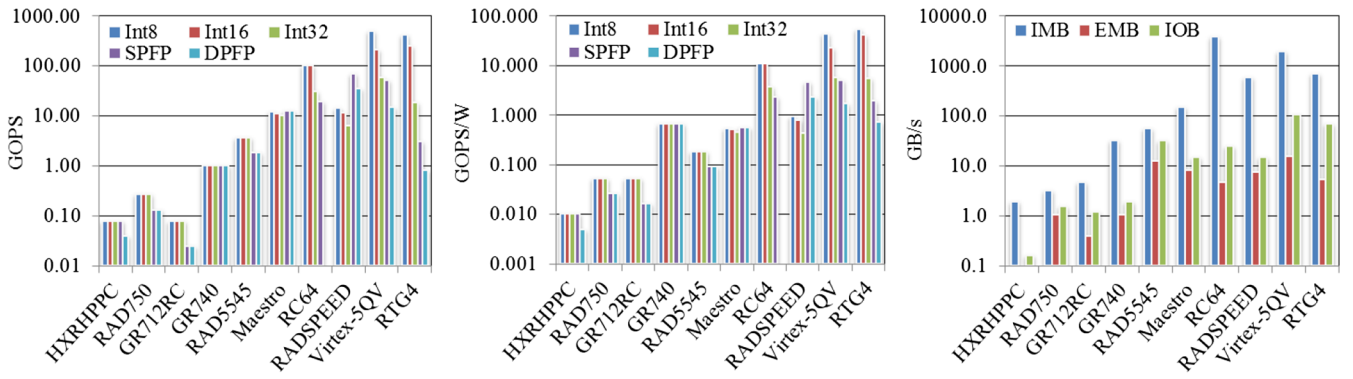
To enable quantitative analysis and objective comparisons of space-grade processors, device metrics are calculated for many diverse space-grade and low-power COTS processors. First, space-grade processors are compared to one another. Next, top-performing space-grade processors are further analyzed to determine how performance varies between applications and kernels based on operations mix. Then, space-grade processors are compared to the closest COTS counterparts upon which they were based to determine the overheads incurred from hardening. Finally, top-performing space-grade and low-power COTS processors are compared to determine the potential for future space-grade processors.

A. Space-Grade Processors

Using the methods described in Sec. III, Fig. 1 provides the CD, CD/W, IMB, EMB, and IOB for various existing and emerging space-grade processors in logarithmic scale, including the Honeywell HXRHPPC™ [28] and BAE Systems RAD750® [29], which are single-core CPUs; the Cobham GR712RC™ [30,31], Cobham GR740™ [32–34], and BAE Systems RAD5545™ [35], which are multicore CPUs; the Boeing Maestro™ [36–38], which is a many-core CPU; the Ramon Chips RC64™ [39–43] and BAE Systems RADSPEED™ [44,45], which are multicore DSPs; and the Xilinx Virtex-5QV FX130 [25–27,46] and Microsemi RTG4™ [47–50], which are FPGAs. Data from Fig. 1 is provided within Table A1.

The HXRHPPC, RAD750, and GR712RC achieve lower CD and CD/W due to slower operating frequencies and older single-core or dual-core CPU architectures with limited computational units. Additionally, they achieve a low IMB due to limited internal caches, a low EMB due to limited or no dedicated external-memory controllers, and a low IOB due to limited and slow input/output resources. CPUs such as the GR740, RAD5545, and Maestro achieve a much higher CD than older CPUs due to their higher operating frequencies, newer multicore and many-core architectures, and (in the case of both the RAD5545 and Maestro), multiple-integer computational units within each processor core. Of all the CPUs compared, the Maestro achieved the highest CD and IMB due to its large number of processor cores and caches, whereas the GR740 achieved the highest CD/W due to its low-power dissipation.

Although the capabilities of space-grade processors are greatly increasing due to newer CPUs, even further gains are made with DSPs and FPGAs. The RC64 achieves a high-integer CD, and the RADSPEED achieves a high floating-point CD due to large levels of parallelism for these types of computational units; and both achieve a high IMB due to large numbers of internal caches and register files. The Virtex-5QV achieves high CD and CD/W, and the RTG4 achieves high-integer CD and CD/W because they support large numbers of computational units at a relatively low-power dissipation; and both achieve a high IMB due to large numbers of internal BRAM units, a high EMB because they support multiple dedicated controllers for external memories, and a high IOB due to the large number of general-purpose input/output ports available.



a) CD b) CD/W c) IMB, EMB, and IOB

Fig. 1 Device metrics data for space-grade processors.

By comparing space-grade processors using device metrics, the changes in capabilities of space-grade processors can be analyzed. The performance achieved by space-grade processors has increased by several orders of magnitude due to newer processors with more advanced architectures that support higher levels of parallelism in terms of computational units, internal memories, and input/output resources.

B. Performance Variations in Space-Grade Processors

The CD calculations for each processor are based upon an operations mix of half-additions and half-multiplications by default because this is a common and critical operations mix for many compute-intensive kernels that are used in space applications. However, a further analysis can be conducted for other important operations mixes. Figure 2 displays several examples of kernels used in space applications and their corresponding operations mixes of additions and multiplications [51–56], where subtractions are considered logically equivalent to additions. Although overheads are required during implementation, these operations mixes characterize the work operations involved, and thus provide a foundation for the performance of each kernel and the applications in which they are used. Figure 3 provides the CD for each top-performing space-grade processor using all possible operations mixes consisting of additions and multiplications in order to demonstrate how the performance varies between different kernels. Data from Fig. 3 is provided within Table A2. Further experimentation would be conducted for additional operations mixes that relate to other kernels consisting of operations such as divisions, shifts, square roots, and trigonometric functions; but, it is not possible because information about the performance of these operations is often not included in vendor-provided documentation or is accomplished using software emulation.

The GR740 contains an integer computational unit for each processor core that can compute one Int8, Int16, or Int32 addition or multiplication per cycle. The GR740 also contains a floating-point computational unit for each processor core that can compute one SPFP or DPFP addition or multiplication per cycle. Therefore, both integer and floating-point CDs remain constant for all operations mixes because additions and multiplications are computed in the same number of cycles.

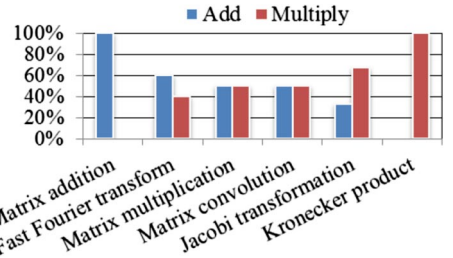
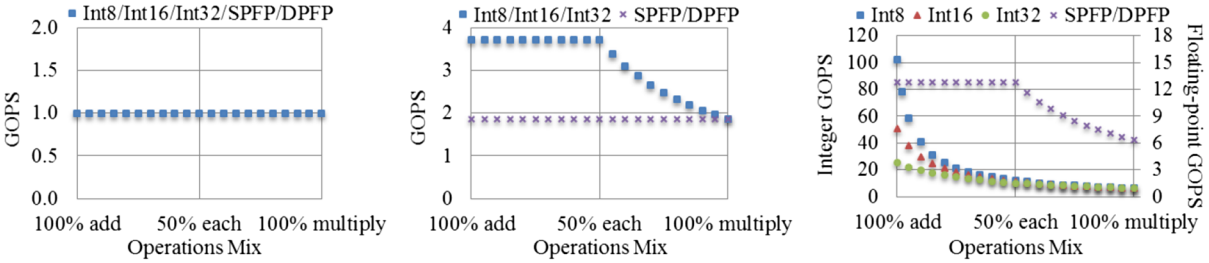
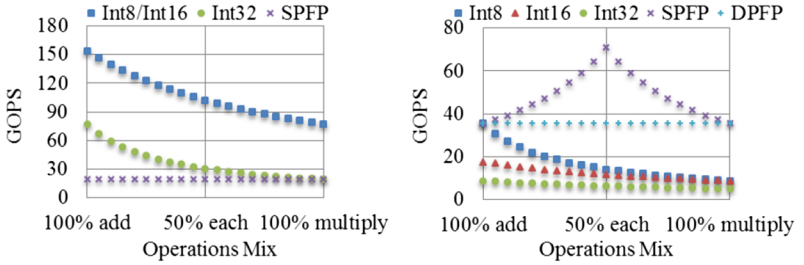


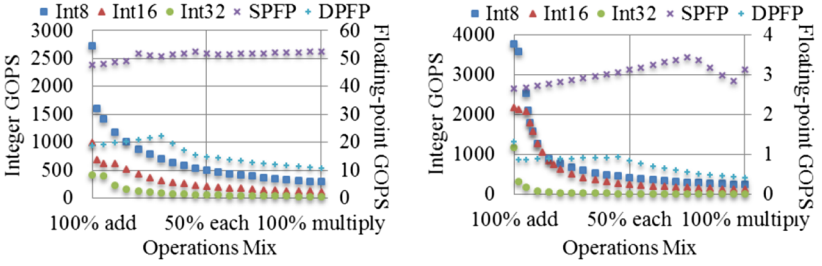
Fig. 2 Operations mixes of compute-intensive kernels.



a) GR740 **b) RAD5545** **c) Maestro**



d) RC64 **e) RADSPEED**



f) Virtex-5QV **g) RTG4**

Fig. 3 Performance variations in space-grade processors.

The RAD5545 contains several integer computational units for each processor core, including two units that can each compute one Int8, Int16, or Int32 addition per cycle and one unit that can compute one Int8, Int16, or Int32 multiplication per cycle. Operations can be issued to two of these units in the same cycle, resulting in the ability to compute both an addition and a multiplication per cycle, two additions per cycle, or one multiplication per cycle. Therefore, the integer CD remains constant for operations mixes with a majority of additions, but it decreases up to 50% as the percentage of multiplications surpasses the percentage of additions due to more multiplications that cannot be computed simultaneously with additions. The RAD5545 also contains a floating-point computational unit for each processor that can compute one SPFP or DPFP addition or multiplication per cycle. Therefore, the floating-point CD remains constant for all operations mixes because additions and multiplications are computed in the same number of cycles.

The Maestro contains several integer computational units for each processor core, including two units that can each compute four Int8 additions, two Int16 additions, or one Int32 addition per cycle, and one unit that can compute one Int8, Int16, or Int32 multiplication in two cycles. Therefore, the integer CD decreases up to 94% as the percentage of multiplications increases because multiplications take more cycles to compute than additions and have less computational units for each processor core. The Maestro also contains a floating-point computational unit for each processor core that can compute one SPFP or DPFP addition per cycle and one SPFP or DPFP multiplication in two cycles, with the ability to interleave additions with multiplications. Therefore, the floating-point CD remains constant for operations mixes with a majority of additions but decreases up to 50% as the percentage of multiplications surpasses the percentage of additions because multiplications take more cycles to compute and this results in more multiplications that cannot be interleaved with additions.

The RC64 contains several computational units for each processor core that can compute eight Int8 or Int16 additions per cycle, four Int32 additions per cycle, four Int8 or Int16 multiplications per cycle, one Int32 multiplication per cycle, or one SPFP addition or multiplication per cycle. DPFP operations are not supported. Therefore, the integer CD decreases up to 75% as the percentage of multiplications increases because multiplications take more cycles to compute than additions. The floating-point CD remains constant for all operations mixes because additions and multiplications are computed in the same number of cycles.

The RADSPEED contains an integer computational unit for each processor core that can compute one Int8 addition per cycle, one Int16 addition in two cycles, one Int32 addition in four cycles, one Int8 or Int16 multiplication in four cycles, or one Int32 multiplication in seven cycles. Therefore, the integer CD decreases up to 75% as the percentage of multiplications increases because multiplications take more cycles to compute than additions. The RADSPEED also contains several floating-point computational units for each processor core, including one unit that can compute one SPFP or DPFP addition per cycle and one unit that can compute one SPFP or DPFP multiplication per cycle. Operations can be issued to both of these units in the same cycle, resulting in the ability to compute both an addition and a multiplication per cycle but not two additions or two multiplications per cycle. However, the ability to compute two operations per cycle only applies to SPFP operations because DPFP operations are limited by bus widths. Therefore, a single-precision floating-point CD peaks when the percentages of additions and multiplications are equal and decreases up to 50% as the percentages of additions and multiplications become more unbalanced. The double-precision floating-point CD remains constant for all operations mixes because additions and multiplications are computed in the same number of cycles.

The Virtex-5QV and RTG4 contain reconfigurable fabrics that support computational units that compute one Int8, Int16, Int32, SPFP, or DPFP addition or multiplication per cycle. As data types and precisions increase, slower operating frequencies can typically be achieved and more logic resources are required. For Int8, Int16, and Int32 operations, multiplications typically achieve slower operating frequencies than additions and require more logic resources. Therefore, the integer CD decreases up to ~92% for the Virtex-5QV and up to ~99% for the RTG4 as the percentage of multiplications increases. For SPFP and DPFP operations, multiplications typically achieve slower operating frequencies than additions and require less logic resources when digital-signal-processing units are used, but they require more logic resources when these units are not used. Therefore, the floating-point CD either increases or decreases as the percentage of multiplications increases, depending on the use of digital-signal-processing units. However, the floating-point CD does not vary as much as the integer CD because the differences between logic resources used for additions and multiplications are not as significant.

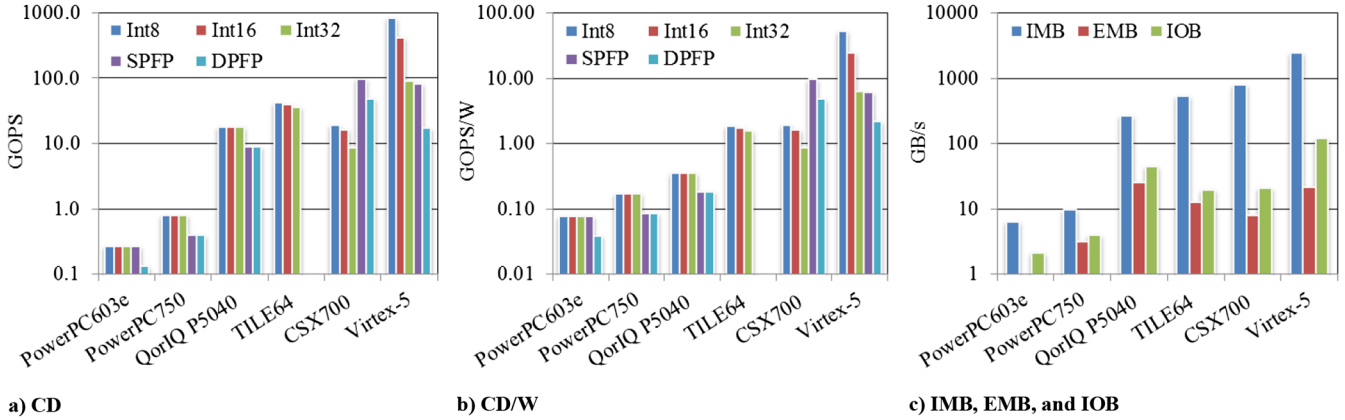
By matching the operations mixes from Fig. 2 with the results from Fig. 3, the variations in performance between different kernels can be analyzed for each top-performing space-grade processor. For all operations on the GR740, the floating-point operations on the RAD5545 and RC64, and the double-precision floating-point operations on the RADSPEED, the CD does not vary between kernels. For integer operations on the RAD5545 and floating-point operations on the Maestro, the CD is highest for kernels that use at least half-additions (such as matrix addition, fast Fourier transform, matrix multiplication, and matrix convolution), becomes worse for kernels that use more than half-multiplications (such as Jacobi transformation), and is lowest for kernels that use all multiplications (such as the Kronecker product). For integer operations on the Maestro, RC64, RADSPEED, Virtex-5QV, and RTG4, the CD is highest for kernels that use all additions such as matrix addition and becomes worse for all other kernels where more multiplications are used. For single-precision floating-point operations on the RADSPEED, the CD is highest for kernels that use half-additions and half-multiplications (such as matrix multiplication and matrix convolution), becomes worse for all other kernels as either more additions or more multiplications are used, and is lowest for kernels that use either all additions or all multiplications (such as matrix addition or the Kronecker product). For floating-point operations on the Virtex-5QV and RTG4, the CD varies moderately between kernels. Variations in the CD demonstrate how the performance of space-grade processors is affected by the operations mixes of compute-intensive kernels used in space applications.

C. Overheads Incurred from Radiation Hardening

Figure 4 provides the CD, CD/W, IMB, EMB, and IOB for the closest COTS counterparts to the space-grade processors from Fig. 1 in logarithmic scale, where the HXRHPPC was based upon the Freescale PowerPC603e™ [57], the RAD750 was based upon the IBM PowerPC750™ [58–60], the RAD5545 was based upon the QorIQ P5040 [21–23], the Maestro was based upon the Tilera TILE64™ [61,62], the RADSPEED was based upon the ClearSpeed CSX700™ [63,64], and the Virtex-5QV FX130 was based upon the Virtex-5 FX130T [24–27]. The GR712RC, GR740, RC64, and RTG4 are not included because they were not based upon any specific COTS devices. Data from Fig. 4 is provided within Table A3.

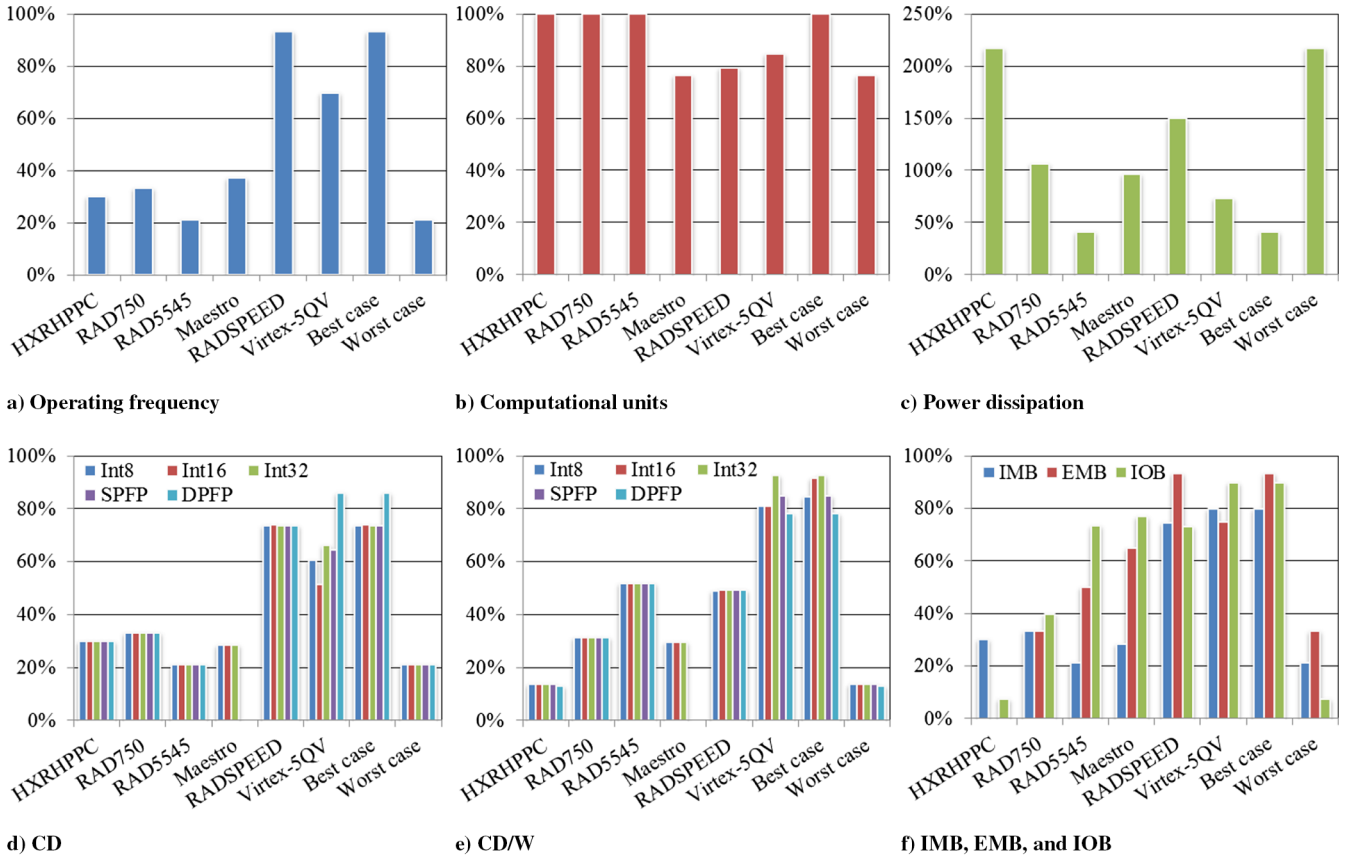
By comparing the results from Figs. 1 and 4, the overheads incurred from hardening of the COTS processors can be calculated. Figure 5 provides the percentages of operating frequencies, the number of computational cores, power dissipation, CD, CD/W, IMB, EMB, and IOB achieved by each space-grade processor as compared to its closest COTS counterpart. Data from Fig. 5 is provided within Tables A4 and A5.

The largest decreases in operating frequencies were for the multicore and many-core CPUs because their closest COTS counterparts benefited from high operating frequencies that were significantly decreased in order to be sustainable on space-grade processors, whereas the closest COTS counterparts to the RADSPEED and Virtex-5QV only required moderate operating frequencies to begin with, and therefore did not need to be decreased as significantly. The largest decreases in the number of computational cores were for the Maestro, RADSPEED, and Virtex-5QV because their closest COTS counterparts contained large levels of parallelism that could not be sustained after hardening, whereas the closest COTS counterparts of the multicore CPUs did not contain enough parallelism to require any decreases to the number of computational cores



a) CD b) CD/W c) IMB, EMB, and IOB

Fig. 4 Device metrics data for closest COTS counterparts to space-grade processors.



a) Operating frequency b) Computational units c) Power dissipation

d) CD e) CD/W f) IMB, EMB, and IOB

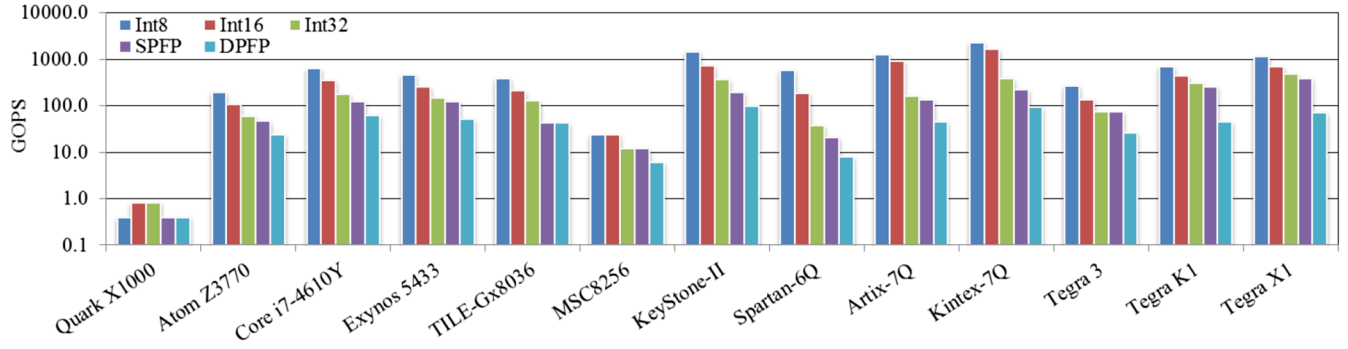
Fig. 5 Percentages achieved by space-grade processors after radiation hardening.

during hardening. The Maestro achieved a larger floating-point CD and CD/W than its closest COTS counterpart due to the addition of floating-point units to each processor core, resulting in the only occurrence of increases in device metrics after radiation hardening. Increases and decreases in power dissipation were more unpredictable because they were dependent on many factors, including decreases in operating frequencies and the number of computational cores and changes to input/output peripherals.

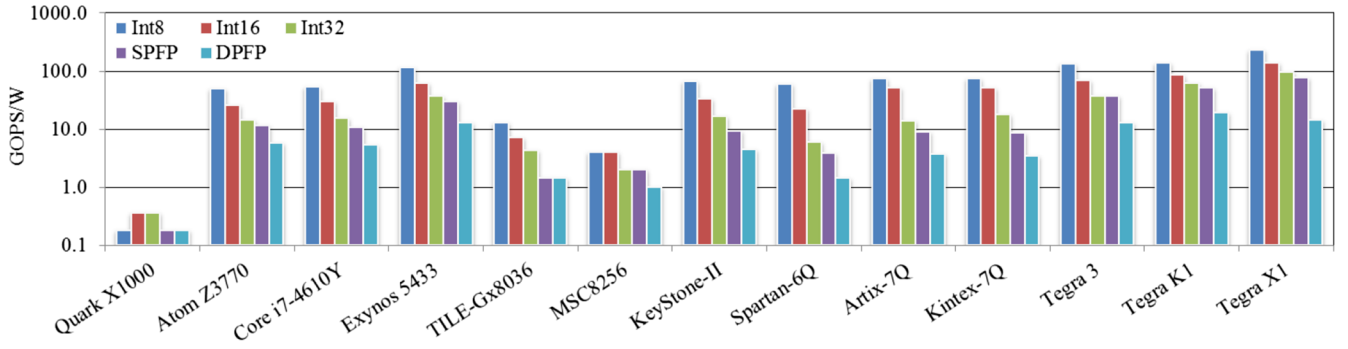
By comparing space-grade processors to their closest COTS counterparts using device metrics, the overheads incurred from hardening can be analyzed. The largest decreases in the CD and IMB occurred for the multicore and many-core CPUs rather than the DSP and FPGA, demonstrating that large decreases in operating frequencies had a more significant impact on the resulting CD and IMB than decreases in the number of computational cores. The smallest decreases in the CD/W occurred for the Virtex-5QV due to relatively small decreases in the CD and only minor variations in power dissipation. The largest decreases in the EMB and IOB occurred for the older single-core CPUs because their input/output resources were highly dependent on operating frequencies that were significantly decreased. These overheads can be considered when analyzing processors for potential hardening and use in space missions.

D. Projected Future Space-Grade Processors

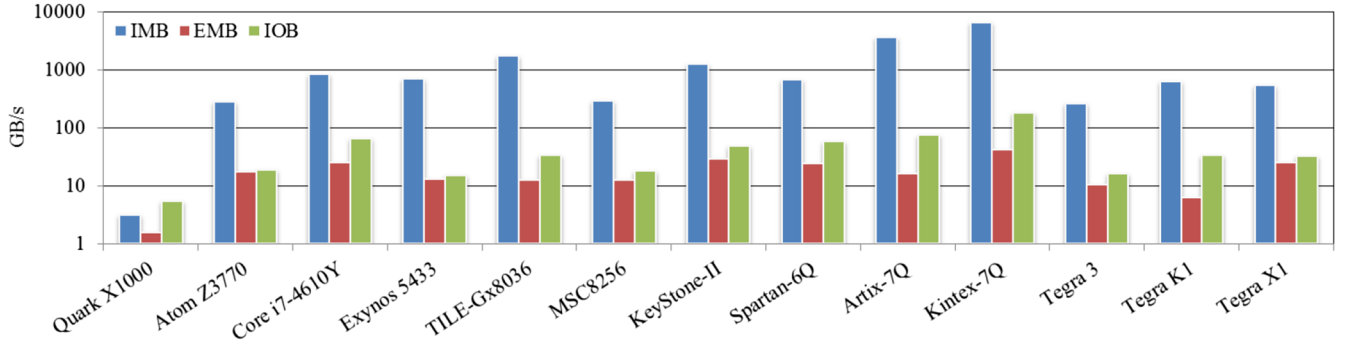
Figure 6 provides the CD, CD/W, IMB, EMB, and IOB for a variety of low-power COTS processors in logarithmic scale, including the Intel Quark™ X1000 [65,66], which is a single-core CPU; the Intel Atom™ Z3770 [67,68], Intel Core™ i7-4610Y [69–72], and Samsung Exynos™ 5433 [73–75], which are multicore CPUs; the Tilera TILE-Gx8036™ [76–78], which is a many-core CPU; the Freescale MSC8256™ [79–81],



a) CD



b) CD/W



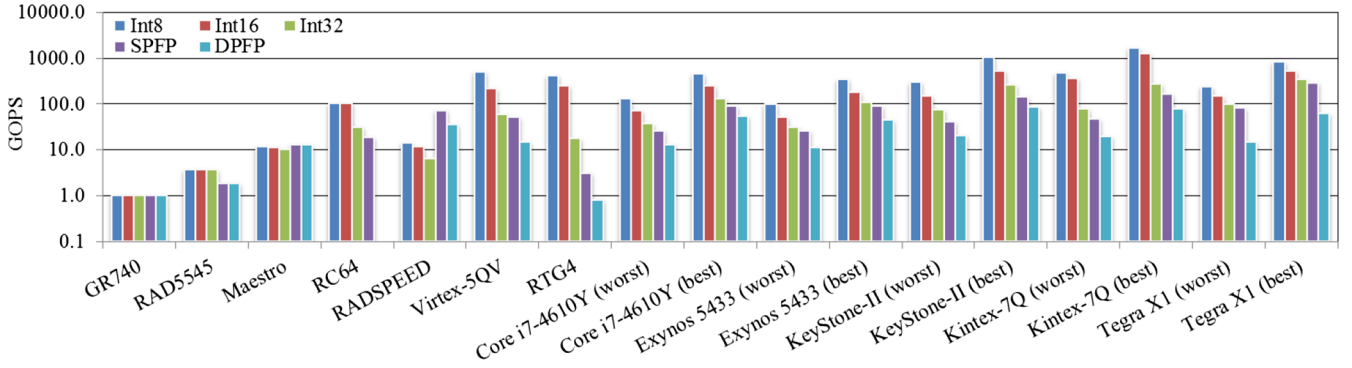
c) IMB, EMB, and IOB

Fig. 6 Device metrics data for low-power COTS processors.

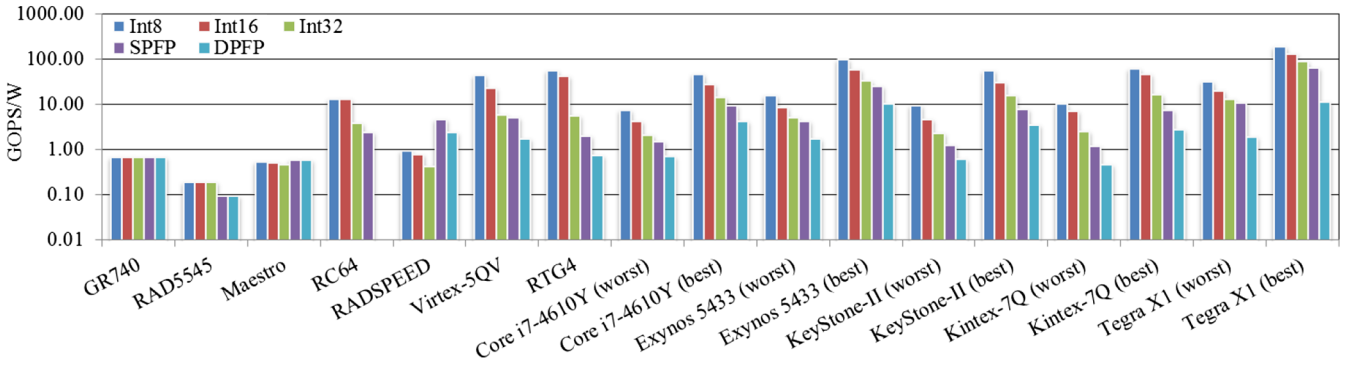
which is a multicore DSP; the Texas Instruments KeyStone™-II 66AK2H12 [82–84], which is a multicore DSP paired with a multicore CPU; the Xilinx Spartan®-6Q LX150T [25,26,85,86], Xilinx Artix®-7Q 350T [25,26,87,88], and Xilinx Kintex®-7Q K410T [25,26,87,88], which are FPGAs; and the NVIDIA Tegra® 3 [89,90], NVIDIA Tegra K1 [83,84,91], and Tegra X1 [74,75,92], which are GPUs paired with multicore CPUs. Several modern processors are considered from each architectural category with power dissipation no larger than 30 W. Data from Fig. 6 is provided within Table A6.

By comparing many low-power COTS processors, the top-performing architectures can be selected and considered for potential hardening and use in future space missions. Although the Core i7-4610Y is the top-performing CPU in most cases, the Exynos 5433 achieves the largest CD/W of the CPUs due to its small power dissipation. The top-performing DSP, FPGA, and GPU are the KeyStone-II, Kintex-7Q, and Tegra X1, respectively. However, if the architectures from these COTS processors were to be used in potential future space-grade processors, several overheads would likely be incurred during the hardening process that must be considered. Therefore, the results for top-performing COTS processors from Fig. 6 are decreased based on the worst-case and best-case hardening overheads from Fig. 5 in order to project device metrics for potential future space-grade processors. Figure 7 provides worst-case and best-case projections in logarithmic scale for potential future space-grade processors based on the Core i7-4610Y, Exynos 5433, KeyStone-II, Kintex-7Q, and Tegra X1 alongside the top-performing space-grade processors from Fig. 1 to determine how additional radiation hardening of top-performing COTS processors could impact the capabilities of space-grade processors. Data from Fig. 7 is provided within Tables A7 and A8.

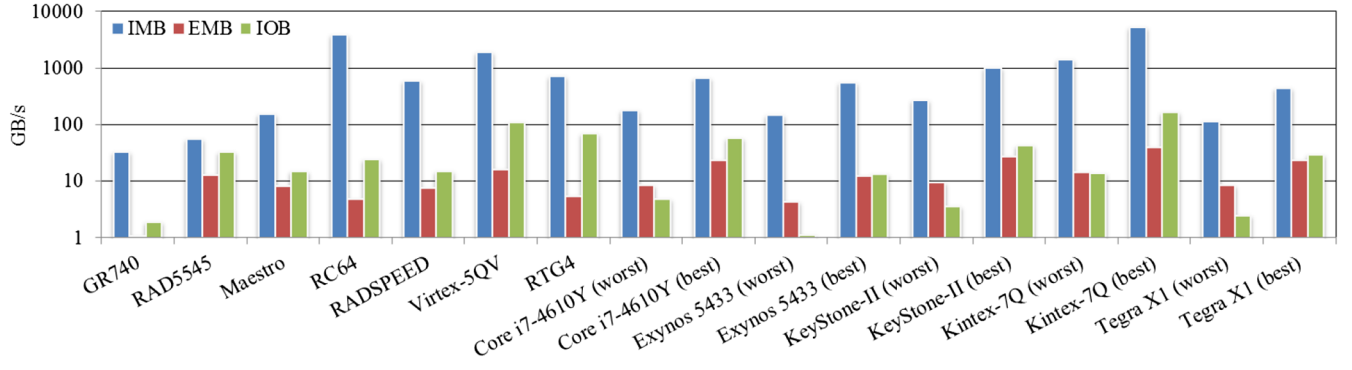
By comparing top-performing and projected future space-grade processors using device metrics, the potential benefits of hardening additional COTS architectures can be analyzed. Although the results from Fig. 5 suggest that the hardening of CPUs typically results in large overheads, the Core i7-4610Y and Exynos 5433 achieve the largest CD and CD/W for each data type considered, as well as the largest IMB, out of all space-grade CPUs even when using worst-case projections. However, the results from Fig. 5 also suggest that the hardening of DSPs and FPGAs typically results in smaller overheads. When using best-case projections, the KeyStone-II and Kintex-7Q achieve the largest CD and CD/W for each data type considered, as well as the largest EMB, as well as the largest IMB and IOB in most cases, out of all space-grade processors. Finally, although there are no past results for the hardening of GPUs, the Tegra X1 achieves a large CD and CD/W and a moderate IMB, EMB, and IOB within the range of projections used. Based on the projections and comparisons from Fig. 7, COTS processors from each architectural category have a high



a) CD



b) CD/W



c) IMB, EMB, and IOB

Fig. 7 Device metrics data for present and projected future space-grade processors.

potential to increase the capabilities of space-grade processors, even with the overheads incurred from hardening. Therefore, as expected, the hardening of modern COTS processors could benefit space computing in terms of performance, power efficiency, memory bandwidth, and input/output bandwidth; and these results help to quantify potential outcomes.

V. Conclusions

As the performance needs for onboard space computing are continually increasing, existing and emerging space-grade and low-power commercial-off-the-shelf (COTS) processors are analyzed for potential use in future space missions. A device metrics analysis is demonstrated as a methodology to quantitatively and objectively analyze a large and diverse set of processor architectures. The results are generated to enable comparisons of space-grade processors to one another, comparisons of space-grade processors to their closest COTS counterparts to determine overheads incurred from radiation hardening, and comparisons of top-performing space-grade and COTS processors to determine the potential for future space-grade processors.

The results demonstrate and quantify how emerging space-grade processors with multicore and many-core CPU, DSP, and FPGA architectures are continually increasing the capabilities of space missions by supporting high levels of parallelism in terms of computational units, internal memories, and input/output resources. In particular, the best results are provided by the RC64, Virtex-5QV, and RTG4 for the integer CD and CD/W; the RADSPEED and Virtex-5QV for the floating-point CD and CD/W; the RC64 and Virtex-5QV for the IMB; the RAD5545 and Virtex-5QV for the EMB; and the RAD5545, Virtex-5QV, and RTG4 for the IOB. Additionally, CD results for each top-performing space-grade processor are further analyzed to demonstrate and evaluate how the performance can vary significantly between applications, depending on the operations mixes used within compute-intensive kernels, with the largest variations occurring for integer operations on the Maestro, Virtex-5QV, and RTG4.

Furthermore, the overheads incurred from radiation hardening were quantified and analyzed, where the overheads incurred by the space-grade CPUs were typically much larger than those incurred by the RADSPEED and Virtex-5QV because they required more significant decreases in operating frequencies. Finally, overheads from past cases of hardening were used to project device metrics for potential future space-grade

processors, demonstrating and quantifying how the hardening of modern COTS processors from each architectural category could result in significant increases in the capabilities of future space missions. In particular, the Core i7-4610Y and Exynos 5433 could provide the largest CD, CD/W, and IMB out of all space-grade CPUs; the KeyStone-II 66AK2H12 and Kintex-7Q K410T could provide the largest CD, CD/W, and EMB out of all space-grade processors, as well as the largest IMB and IOB in most cases; and the Tegra X1 could provide the largest CD and CD/W out of all space-grade processors, as well as moderate IMB, EMB, and IOB.

By using device metrics to analyze and compare present and future space-grade processors, tradeoffs between architectures were determined and could be considered when comparing or designing processors for future space missions. Future research directions will involve optimized device benchmarking of top-performing space-grade processors to analyze and optimize their performance capabilities for key space applications and kernels.

Appendix: Device Metrics Data

Table A1 Device metrics data for space-grade processors

	CD (GOPS)						CD/W (GOPS/W)							
Processor	Int8	Int16	Int32	SPFP	DPFP	Power (W)	Int8	Int16	Int32	SPFP	DPFP	IMB (GB/s)	EMB (GB/s)	IOB (GB/s)
Honeywell HXRHPPC	0.08	0.08	0.08	0.08	0.04	7.60	0.01	0.01	0.01	0.01	0.01	1.92	0.00	0.16
BAE Systems RAD750	0.27	0.27	0.27	0.13	0.13	5.00	0.05	0.05	0.05	0.03	0.03	3.19	1.06	1.59
Cobham GR712RC	0.08	0.08	0.08	0.03	0.03	1.50	0.05	0.05	0.05	0.02	0.02	4.80	0.40	1.21
Cobham GR740	1.00	1.00	1.00	1.00	1.00	1.50	0.67	0.67	0.67	0.67	0.67	32.80	1.06	1.90
BAE Systems RAD5545	3.73	3.73	3.73	1.86	1.86	20.00	0.19	0.19	0.19	0.09	0.09	55.58	12.80	32.48
Boeing Maestro	11.99	11.32	10.19	12.74	12.74	22.20	0.54	0.51	0.46	0.57	0.57	152.88	8.32	15.07
Ramon Chips RC64	102.40	102.40	30.72	19.20	0.00	8.00	12.80	12.80	3.84	2.40	0.00	3840.00	4.80	24.80
BAE Systems RADSPEED	14.17	11.81	6.44	70.83	35.42	15.00	0.94	0.79	0.43	4.72	2.36	589.04	7.46	15.16
Xilinx Virtex-5QV FX130	503.72	214.57	59.67	51.93	14.96	9.97[a]	44.30	22.62	5.91	5.14	1.70	1931.04	16.00	109.16
Microsemi RTG4	418.32	252.18	18.36	3.12	0.83	3.91[b]	55.60	41.71	5.68	1.96	0.74	707.40	5.33	68.70

[a]Averaged between data types (Int8: 11.37 W; Int16: 9.49 W; Int32: 10.09 W; SPFP: 10.10 W; DPFP: 8.78 W).
[b]Averaged between data types (Int8: 7.52 W; Int16: 6.05 W; Int32: 3.23 W; SPFP: 1.60 W; DPFP: 1.14 W).

Table A2 Performance variations in space-grade processors

	CD for 100% add (GOPS)					CD for 50% add, 50% multiply (GOPS)					CD for 100% multiply (GOPS)				
Processor	Int8	Int16	Int32	SPFP	DPFP	Int8	Int16	Int32	SPFP	DPFP	Int8	Int16	Int32	SPFP	DPFP
Cobham GR740	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
BAE Systems RAD5545	3.73	3.73	3.73	1.86	1.86	3.73	3.73	3.73	1.86	1.86	1.86	1.86	1.86	1.86	1.86
Boeing Maestro	101.92	50.96	25.48	12.74	12.74	11.99	11.32	10.19	12.74	12.74	6.37	6.37	6.37	6.37	6.37
Ramon Chips RC64	153.60	153.60	76.80	19.20	0.00	102.40	102.40	30.72	19.20	0.00	76.80	76.80	19.20	19.20	0.00
BAE Systems RADSPEED	35.42	17.71	8.85	35.42	35.42	14.17	11.81	6.44	70.83	35.42	8.85	8.85	5.06	35.42	35.42
Xilinx Virtex-5QV FX130	2722.86	988.42	413.12	47.65	18.72	503.72	214.57	59.67	51.93	14.96	293.83	117.01	33.15	52.47	10.66
Microsemi RTG4	3766.97	2180.88	1169.23	2.64	1.32	418.32	252.18	18.36	3.12	0.83	238.66	126.09	9.42	3.12	0.42

Table A3 Device metrics data for closest COTS counterparts to space-grade processors

	CD (GOPS)						CD/W (GOPS/W)							
Processor	Int8	Int16	Int32	SPFP	DPFP	Power (W)	Int8	Int16	Int32	SPFP	DPFP	IMB (GB/s)	EMB (GB/s)	IOB (GB/s)
Freescale PowerPC603e	0.27	0.27	0.27	0.27	0.13	3.50	0.08	0.08	0.08	0.08	0.04	6.38	0.00	2.13
IBM PowerPC750	0.80	0.80	0.80	0.40	0.40	4.70	0.17	0.17	0.17	0.09	0.09	9.60	3.20	4.00
Freescale QorIQ P5040	17.60	17.60	17.60	8.80	8.80	49.00	0.36	0.36	0.36	0.18	0.18	262.40	25.60	44.22
Tilera TILE64	42.16	39.82	35.84	0.00	0.00	23.00	1.83	1.73	1.56	0.00	0.00	537.60	12.80	19.55
ClearSpeed CSX700	19.20	16.00	8.73	96.00	48.00	10.00	1.92	1.60	0.87	9.60	4.80	792.00	8.00	20.72
Xilinx Virtex-5 FX130T	833.20	416.00	89.97	80.52	17.43	13.61[a]	52.50	24.72	6.39	6.06	2.18	2413.80	21.33	121.58

[a]Averaged between data types (Int8: 15.87 W; Int16: 16.83 W; Int32: 14.07 W; SPFP: 13.28 W; DPFP: 8.00 W).

Table A4 Radiation-hardening outcomes for space-grade processors

	Space grade			Closest COTS counterpart			Percentages achieved by space grade		
Processor	Operating frequency (GHz)	Computational cores	Power (W)	Operating frequency (GHz)	Computational cores	Power (W)	Operating frequency (%)	Computational cores (%)	Power (%)
Honeywell HXRHPPC	0.080	1	7.60	0.266	1	3.50	30.08	100.00	217.14
BAE Systems RAD750	0.133	1	5.00	0.400	1	4.70	33.25	100.00	106.38
BAE Systems RAD5545	0.466	4	20.00	2.200	4	49.00	21.18	100.00	40.82
Boeing Maestro	0.260	49	22.20	0.700	64	23.00	37.14	76.56	96.52
BAE Systems RADSPEED	0.233	76	15.00	0.250	96	10.00	93.20	79.17	150.00
Xilinx Virtex-5QV FX130	0.259[a]	695[a]	9.97[a]	0.371[b]	820[b]	13.61[b]	69.83	84.79	73.22

[a]Averaged between data types (Int8: 0.301 GHz, 1672 cores, 11.37 W; Int16: 0.206 GHz, 1043 cores, 9.49 W; Int32: 0.216 GHz, 276 cores, 10.09 W; SPFP: 0.223 GHz, 233 cores, 10.10 W; DPFP: 0.187 GHz, 79 cores, 8.78 W).
[b]Averaged between data types (Int8: 0.353 GHz, 2358 cores, 15.87 W; Int16: 0.381 GHz, 1092 cores, 16.83 W; Int32: 0.302 GHz, 298 cores, 14.07 W; SPFP: 0.327 GHz, 246 cores, 13.28 W; DPFP: 0.161 GHz, 108 cores, 8.00 W).

Table A5 Percentages achieved by space-grade processors after radiation hardening

	CD (%)					CD/W (%)							
Processor	Int8	Int16	Int32	SPFP	DPFP	Int8	Int16	Int32	SPFP	DPFP	IMB (%)	EMB (%)	IOB (%)
Honeywell HXRHPPC	30.08	30.08	30.08	30.08	30.08	13.85	13.85	13.85	13.85	13.16	30.08	[a]	7.52
BAE Systems RAD750	33.25	33.25	33.25	33.25	33.25	31.26	31.26	31.26	31.26	31.26	33.25	33.25	39.80
BAE Systems RAD5545	21.18	21.18	21.18	21.18	21.18	51.90	51.90	51.90	51.90	51.90	21.18	50.00	73.46
Boeing Maestro	28.44	28.44	28.44	[a]	[a]	29.46	29.46	29.46	[a]	[a]	28.44	65.00	77.08
BAE Systems RADSPEED	73.80	73.81	73.77	73.78	73.78	48.96	49.38	49.43	49.19	49.19	74.37	93.25	73.17
Xilinx Virtex-5QV FX130	60.46	51.58	66.32	64.49	85.83	84.39	91.50	92.55	84.85	78.17	80.00	75.00	89.78

[a]Not applicable because original value was zero.

Table A6 Device metrics data for low-power COTS processors

	CD (GOPS)						CD/W (GOPS/W)							
Processor	Int8	Int16	Int32	SPFP	DPFP	Power (W)	Int8	Int16	Int32	SPFP	DPFP	IMB (GB/s)	EMB (GB/s)	IOB (GB/s)
Intel Quark X1000	0.40	0.80	0.80	0.40	0.40	2.22	0.18	0.36	0.36	0.18	0.18	3.20	1.60	5.41
Intel Atom Z3770	198.56	105.12	58.40	46.72	23.36	4.00	49.64	26.28	14.60	11.68	5.84	280.32	17.36	18.79
Intel Core i7-4610Y	626.60	348.20	177.00	124.80	62.40	11.50	54.49	30.28	15.39	10.85	5.43	835.20	25.60	64.10
Samsung Exynos 5433	461.60	251.90	147.20	121.60	52.40	4.00	115.40	62.98	36.80	30.40	13.10	696.00	13.20	15.02
Tilera TILE-Gx8036	388.80	216.00	129.60	43.20	43.20	30.00	12.96	7.20	4.32	1.44	1.44	1728.00	12.80	33.86
Freescale MSC8256	24.00	24.00	12.00	12.00	6.00	6.04	3.97	3.97	1.99	1.99	0.99	288.00	12.80	17.94
TI KeyStone-II 66AK2H12	1459.20	729.60	364.80	198.40	99.20	21.69	67.28	33.64	16.82	9.15	4.57	1270.40	28.80	48.22
Xilinx Spartan -6Q LX150T	590.40	185.10	37.96	21.22	7.86	7.04[a]	60.58	22.46	5.95	3.89	1.47	675.36	24.00	57.80
Xilinx Artix-7Q 350T	1245.00	939.10	163.30	134.20	45.52	14.70[b]	75.49	52.65	13.73	8.93	3.72	3598.61	16.00	75.60
Xilinx Kintex-7Q K410T	2295.00	1696.00	380.60	224.30	91.95	27.41[c]	74.28	51.36	18.03	8.72	3.50	6555.27	42.67	184.29
NVIDIA Tegra 3	265.98	137.98	73.98	73.98	25.60	2.00	132.99	68.99	36.99	36.99	12.80	265.60	10.68	16.33
NVIDIA Tegra K1	697.60	440.00	311.20	256.00	44.40	5.00	139.50	88.00	62.20	51.20	19.52	625.60	6.40	33.58
NVIDIA Tegra X1	1152.00	704.00	480.00	384.00	72.00	5.00	230.40	140.80	96.00	76.80	14.40	544.00	25.60	32.16

[a]Averaged between data types (Int8: 9.75 W; Int16: 8.24 W; Int32: 6.38 W; SPFP: 5.46 W; DPFP: 5.36 W).
[b]Averaged between data types (Int8: 16.49 W; Int16: 17.84 W; Int32: 11.89 W; SPFP: 15.03 W; DPFP: 12.23 W).
[c]Averaged between data types (Int8: 30.90 W; Int16: 33.02 W; Int32: 21.11 W; SPFP: 25.74 W; DPFP: 26.27 W).

Table A7 Device metrics data for projected future space-grade processors (worst case)

	CD (GOPS)					CD/W (GOPS/W)							
Processor	Int8	Int16	Int32	SPFP	DPFP	Int8	Int16	Int32	SPFP	DPFP	IMB (GB/s)	EMB (GB/s)	IOB (GB/s)
Intel Core i7-4610Y	132.73	73.76	37.49	26.43	13.22	7.55	4.19	2.13	1.50	0.71	176.91	8.51	4.82
Samsung Exynos 5433	97.78	53.36	31.18	25.76	11.10	15.98	8.72	5.10	4.21	1.72	147.43	4.39	1.13
TI KeyStone-II 66AK2H12	309.09	154.54	77.27	42.02	21.01	9.32	4.66	2.33	1.27	0.60	269.09	9.58	3.63
Xilinx Kintex-7Q K410T	486.12	359.24	80.62	47.51	19.48	10.29	7.11	2.50	1.21	0.46	1388.52	14.19	13.86
NVIDIA Tegra X1	244.01	149.12	101.67	81.34	15.25	31.91	19.50	13.30	10.64	1.89	115.23	8.51	2.42

Table A8 Device metrics data for projected future space-grade processors (best case)

	CD (GOPS)					CD/W (GOPS/W)							
Processor	Int8	Int16	Int32	SPFP	DPFP	Int8	Int16	Int32	SPFP	DPFP	IMB (GB/s)	EMB (GB/s)	IOB (GB/s)
Intel Core i7-4610Y	462.44	257.02	130.57	92.08	53.56	45.98	27.71	14.24	9.21	4.24	668.16	23.87	57.55
Samsung Exynos 5433	340.67	185.93	108.59	89.72	44.97	97.38	57.63	34.06	25.79	10.24	556.80	12.31	13.49
TI KeyStone-II 66AK2H12	1076.92	538.54	269.11	146.39	85.14	56.78	30.78	15.57	7.76	3.57	1016.32	26.86	43.29
Xilinx Kintex-7Q K410T	1693.76	1251.86	280.76	165.50	78.92	62.68	47.00	16.69	7.39	2.74	5244.21	39.79	165.46
NVIDIA Tegra X1	850.20	519.64	354.09	283.33	61.80	194.43	128.84	88.85	65.17	11.26	435.20	23.87	28.87

Acknowledgments

This work was supported in part by the Industry/University Cooperative Research Center Program of the National Science Foundation under grant nos. EEC-0642422 and IIP-1161022, by the industry and government members of the Center for High-Performance Reconfigurable Computing, and by Xilinx and Microsemi for provided software tools.

References

[1] Lovelly, T. M., and George, A. D., "Comparative Analysis of Present and Future Space Processors," *Proceedings of the Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, Defense Technical Information Center, Ft. Belvoir, VA, March 2015, pp. 1–27.

[2] Lovelly, T. M., Cheng, K., Garcia, W., Bryan, D., Wise, T., and George, A. D., "Device Metrics and Benchmarking Analysis of Next-Generation Architectures for Space Computing," *Proceedings of the 7th Workshop on Fault-Tolerant Spaceborne Computing Employing New Technologies*, Sandia National Labs., Albuquerque, NM, June 2014, pp. 1–27.

[3] Lovelly, T. M., Cheng, K., Garcia, W., and George, A. D., "Comparative Analysis of Present and Future Space Processors with Device Metrics," *Proceedings of the Military and Aerospace Programmable-Logic Devices Conference (MAPLD)*, SEE Symposium, San Diego, CA, May 2014, pp. 1–24.

[4] Doyle, R., Some, R., Powell, W., Mounce, G., Goforth, M., Horan, S., and Lowry, M., "High Performance Spaceflight Computing; Next-Generation Space Processor: A Joint Investment of NASA and AFRL," *Proceedings of the International Symposium on Artificial Intelligence, Robotics, and Automation in Space (i-SAIRAS)*, Canadian Space Agency, Montreal, June 2014, http://robotics.estec.esa.int/i-SAIRAS/isairas2014/Data/Plenaries/ISAIRAS_FinalPaper_0153.pdf [retrieved 2017].

[5] Lovelly, T. M., Bryan, D., Cheng, K., Kreynin, R., George, A. D., Gordon-Ross, A., and Mounce, G., "A Framework to Analyze Processor Architectures for Next-Generation On-Board Space Computing," *Proceedings of the IEEE Aerospace Conference (AERO)*, IEEE, Piscataway, NJ, March 2014, Paper 2440. doi:10.1109/AERO.2014.6836387

[6] Some, R., Doyle, R., Bergman, L., Whitaker, W., Powell, W., Johnson, M., Goforth, M., and Lowry, M., "Human and Robotic Mission Use Cases for High-Performance Spaceflight Computing," *AIAA Infotech@Aerospace Conference (I@A)*, AIAA Paper 2013-4729, Aug. 2013. doi:10.2514/6.2013-4729

[7] Williams, J., Massie, C., George, A. D., Richardson, J., Gosrani, K., and Lam, H., "Characterization of Fixed and Reconfigurable Multi-Core Devices for Application Acceleration," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, Vol. 3, No. 4, Nov. 2010, pp. 1–29. doi:10.1145/1862648

[8] Richardson, J., Fingulin, S., Raghunathan, D., Massie, C., George, A. D., and Lam, H., "Comparative Analysis of HPC and Accelerator Devices: Computation, Memory, I/O, and Power," *Proceedings of the High-Performance Reconfigurable Computing Technology and Applications Workshop (HPRCTA) at ACM/IEEE Supercomputing Conference (SC)*, CFP1015F-ART, IEEE, Piscataway, NJ, Nov. 2010. doi:10.1109/HPRCTA.2010.5670797

[9] Wulf, N., Richardson, J., and George, A. D., "Optimizing FPGA Performance, Power, and Dependability with Linear Programming," *Proceedings of the Military and Aerospace Programmable-Logic Devices Conference (MAPLD)*, SEE Symposium, San Diego, CA, April 2013, pp. 1–13.

[10] Wulf, N., George, A. D., and Gordon-Ross, A., "A Framework for Evaluating and Optimizing FPGA-Based SoCs for Aerospace Computing," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, Vol. 10, No. 1, Dec. 2016, pp. 1–29. doi:10.1145/3002131

[11] Bourdarie, S., and Xapsos, M., "The Near-Earth Space Radiation Environment," *IEEE Transactions on Nuclear Science*, Vol. 55, No. 4, Aug. 2008, pp. 1810–1832. doi:10.1109/TNS.2008.2001409

[12] Barth, J. L., Dyer, C. S., and Stassinopoulos, E. G., "Space, Atmospheric, and Terrestrial Radiation Environments," *IEEE Transactions on Nuclear Science*, Vol. 50, No. 3, June 2003, pp. 466–482. doi:10.1109/TNS.2003.813131

[13] Schwank, J. R., Ferlet-Cavrois, V., Shaneyfelt, M. R., Paillet, P., and Dodd, P. E., "Radiation Effects in SOI Technologies," *IEEE Transactions on Nuclear Science*, Vol. 50, No. 3, June 2003, pp. 522–538. doi:10.1109/TNS.2003.812930

[14] Gaillardin, M., Raine, M., Paillet, P., Martinez, M., Marcandella, C., Girard, S., Duhamel, O., Richard, N., Andrieu, F., Barraud, S., and Faynot, O., "Radiation Effects in Advanced SOI Devices: New Insights into Total Ionizing Dose and Single-Event Effects," *Proceedings of the IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, CFP13SOI-USB, IEEE, Piscataway, NJ, Oct. 2013. doi:10.1109/S3S.2013.6716530

[15] Baumann, R., "Soft Errors in Advanced Computer Systems," *IEEE Design and Test of Computers*, Vol. 22, No. 3, June 2005, pp. 258–266. doi:10.1109/MDT.2005.69

[16] Ballast, J., Amort, T., Cabanas-Holmen, M., Cannon, E. H., Brees, R., Neathery, C., Fischer, S., and Snapp, W., "A Method for Efficient Radiation Hardening of Multicore Processors," *Proceedings of the IEEE Aerospace Conference (AERO)*, IEEE, Piscataway, NJ, March 2015. doi:10.1109/AERO.2015.7119216

[17] Makihara, A., Midorikawa, M., Yamaguchi, T., Iide, Y., Yokose, T., Tsuchiya, Y., Arimitsu, T., Asai, H., Shindou, H., Kuboyama, S., and Matsuda, S., "Hardness-By-Design Approach for 0.15 μm Fully Depleted CMOS/SOI Digital Logic Devices with Enhanced SEU/SET Immunity," *IEEE Transactions on Nuclear Science*, Vol. 52, No. 6, Dec. 2005, pp. 2524–2530. doi:10.1109/TNS.2005.860716

[18] Lacoe, R. C., Osborn, J. V., Koga, R., Brown, S., and Mayer, D. C., "Application of Hardness-By-Design Methodology to Radiation-Tolerant ASIC Technologies," *IEEE Transactions on Nuclear Science*, Vol. 47, No. 6, Dec. 2000, pp. 2334–2341. doi:10.1109/23.903774

[19] Glein, R., Rittner, F., Becher, A., Ziener, D., Frickel, J., Teich, J., and Heuberger, A., "Reliability of Space-Grade vs. COTS SRAM-Based FPGA in N-Modular Redundancy," *NASA/ESA Adaptive Hardware and Systems Conference (AHS)*, CFP1563A-ART, IEEE, Piscataway, NJ, June 2015. doi:10.1109/AHS.2015.7231159

[20] Ginosar, R., "Survey of Processors for Space," *Proceedings of the Data Systems in Aerospace Conference (DASIA)*, AeroSpace and Defence Industries Association of Europe, ESA SP-701, Dubrovnik, Croatia, May 2012, http://www.ramon-chips.com/papers/SurveySpaceProcessors-DASIA2012-paper.pdf [retrieved 2017].

[21] e5500 Core Reference Manual, Rev. 4, Freescale Semiconductor, Austin, TX, March 2013, pp. 36–46, 151–152, 162, 246–250, 274, https://www.nxp.com/webapp/Download?colCode=E5500RM.

[22] "P5040 QorIQ Integrated Processor Data Sheet," Rev. 1, Freescale Semiconductor, Austin, TX, May 2014, http://cache.freescale.com/files/32bit/doc/data_sheet/P5040.pdf [retrieved 03 July 2016].

[23] P5040 QorIQ Integrated Multicore Communication Processor Reference Manual, Rev. 3, Freescale Semiconductor, Austin, TX, June 2016, pp. 65–76, 128–138.

[24] "Virtex-5 Family Overview: DS100 (v5.1)," Xilinx, Inc., Product Specification, San Jose, CA, Aug. 2015, https://www.xilinx.com/support/documentation/data_sheets/ds100.pdf [retrieved 2017].

[25] "LogiCORE IP CORDIC v4.0: DS249," Xilinx Inc., Product Specification, San Jose, CA, March 2011, https://www.xilinx.com/support/documentation/ip_documentation/cordic_ds249.pdf [retrieved 2017].

[26] "LogiCORE IP Floating-Point Operator v5.0: DS335," Xilinx Inc., Product Specification, San Jose, CA, March 2011, https://www.xilinx.com/support/documentation/ip_documentation/floating_point_ds335.pdf [retrieved 2017].

[27] "Xilinx Power Estimator: Virtex-5, Virtex-6: XPE 14.3," Xilinx Inc., San Jose, CA, Oct. 2012, https://www.xilinx.com/products/technology/power/xpe.html [retrieved 2017].

[28] "HXRHPPC Rad Hard Microprocessor," Honeywell International, Inc., Form 900378, Plymouth, MN, Aug. 2008, https://www.xilinx.com/products/technology/power/xpe/license-virtex-5-virtex-6.html [retrieved 2017].

[29] Berger, R. W., Bayles, D., Brown, R., Doyle, S., Kazemzadeh, A., Knowles, K., Moser, D., Rodgers, J., Saari, B., and Stanley, D., "The RAD750—A Radiation Hardened PowerPC Processor for High Performance Spaceborne Applications," *Proceedings of the IEEE Aerospace Conference (AERO)*, IEEE, Piscataway, NJ, March 2001. doi:10.1109/AERO.2001.931184

[30] "LEON3-FT SPARC V8 Processor LEON3FT-RTAX Data Sheet and User's Manual," LEON3FT-RTAX Ver. 1.9, Cobham/Gaisler, Göteborg, Sweden, Jan. 2013, pp. 1–2, 15–17, 28, 32–33, http://www.gaisler.com/doc/leon3ft-rtax-ag.pdf [retrieved 2017].

[31] "GR712RC: Dual-Core LEON3-FT SPARC V8 Processor," GR712RC-DS Ver. 2.3, Cobham/Gaisler, Göteborg, Sweden, Jan. 2016, http://www.gaisler.com/j25/doc/gr712rc-datasheet.pdf [retrieved 2017].

[32] "GR740: Quad-Core LEON4 SPARC V8 Processor," GR740-UM-DS, Ver. 1.5, Cobham/Gaisler, Göteborg, Sweden, Nov. 2016, http://www.gaisler.com/doc/gr740/GR740-UM-DS.pdf [retrieved 2017].

[33] Hjorth, M., Aberg, M., Wessman, N., Andersson, J., Chevallier, R., Forsyth, R., Weigand, R., and Fossati, L., "GR740: Rad-Hard Quad-Core LEON4FT System-on-Chip," *Proceedings of the Data Systems in Aerospace Conference (DASIA)*, AeroSpace and Defence Industries Association of Europe, ESA SP-732, Barcelona, May 2015, http://microelectronics.esa.int/ngmp/DASIA2015-GR740-Hjorth.pdf [retrieved 2017].
[34] Andersson, J., Hjorth, M., Habinc, S., and Gaisler, J., "Development of a Functional Prototype of the Quad Core NGMP Space Processor," *Proceedings of Data Systems in Aerospace Conference (DASIA)*, AeroSpace and Defence Industries Association of Europe, ESA SP-701, Dubrovnik, Croatia, May 2012, http://microelectronics.esa.int/ngmp/NGMP-NGFP-DASIA-2012-Paper.pdf [retrieved 2017].
[35] Berger, R., et al., "Quad-Core Radiation-Hardened System-On-Chip Power Architecture Processor," *Proceedings of the IEEE Aerospace Conference (AERO)*, IEEE, Piscataway, NJ, March 2015.
doi:10.1109/AERO.2015.7119114
[36] Rogers, C. M., Barnhart, D., and Crago, S., "The Maestro Flight Experiment: A 49-Core Radiation Hardened Processor in Space," *Proceedings of the IEEE Aerospace Conference (AERO)*, IEEE, Piscataway, NJ, March 2016.
doi:10.1109/AERO.2016.7500626
[37] Suh, J., Kang, D. I. D., and Crago, S. P., "Implementation of Kernels on the Maestro Processor," *Proceedings of the IEEE Aerospace Conference (AERO)*, CFP13AAC·CDR, IEEE, Piscataway, NJ, March 2013.
doi:10.1109/AERO.2013.6496949
[38] Villalpando, C., Rennels, D., Some, R., and Cabanas-Holmen, M., "Reliable Multicore Processors for NASA Space Missions," *Proceedings of the IEEE Aerospace Conference (AERO)*, IEEE, Piscataway, NJ, March 2011.
doi:10.1109/AERO.2011.5747447
[39] Ginosar, R., Aviely, P., Israeli, T., and Meirov, H., "RC64: High Performance Rad-Hard Manycore," *Proceedings of the IEEE Aerospace Conference (AERO)*, IEEE, Piscataway, NJ, March 2016.
doi:10.1109/AERO.2016.7500697
[40] Ginosar, R., Aviely, P., Lange, F., and Liran, T., "RC64: High Performance Rad-Hard Manycore with FPGA Extension for Telecomm Satellites and Other Space Applications," *Proceedings of the Military and Aerospace Programmable-Logic Devices Conference (MAPLD)*, SEE Symposium, San Diego, CA, May 2015, pp. 1–4, http://www.ramon-chips.com/papers/MAPLD2015-RC64-paper.pdf [retrieved 2017].
[41] Ginosar, R., Aviely, P., Gellis, H., Liran, T., Israeli, T., Nesher, R., Lange, F., Dobkin, R., Meirov, H., and Reznik, D., "A Rad-Hard Many-Core High-Performance DSP for Space Applications," *Proceedings of the Data Systems in Aerospace Conference (DASIA)*, AeroSpace and Defence Industries Association of Europe, ESA SP-732, Barcelona, May 2015, http://www.ramon-chips.com/papers/DASIA2015-RC64-paper.pdf [retrieved 2017].
[42] Byrne, J., "Ceva Trains DSP Guns on TI: Ceva Coaxes Designers to Move to Its Ceva-X and Ceva-XC DSP IP," Linley Newsletter, No. 331, 11 Nov. 2010, http://linleygroup.com/newsletters/newsletter_detail.php?num=3993 [retrieved 2017].
[43] Balaish, E., "Architecture Oriented C Optimizations, Part 1: DSP Features," EE Times, 27 Aug. 2008, http://www.eetimes.com/document.asp?doc_id=1275609 [retrieved 2017].
[44] Marshall, J., Berger, R., Bear, M., Hollinden, L., Robertson, J., and Rickard, D., "Applying a High Performance Tiled Rad-Hard Digital Signal Processor to Spaceborne Applications," *Proceedings of the IEEE Aerospace Conference (AERO)*, IEEE, Piscataway, NJ, March 2012.
doi:10.1109/AERO.2012.6187229
[45] Marshall, J. R., Bear, M., Hollinden, L., and Lapihuska, R., "Emergence of a High Performance Tiled Rad-Hard Digital Signal Processor for Spaceborne Applications," *AIAA Infotech@Aerospace Conference (I@A)*, AIAA Paper 2013-4728, Aug. 2013.
doi:10.2514/6.2013-4728
[46] "Radiation-Hardened, Space-Grade Virtex-5QV Family Overview: DS192 (v1.4)," Xilinx Inc., San Jose, CA, Nov. 2014, https://www.xilinx.com/support/documentation/data_sheets/ds192_V5QV_Device_Overview.pdf [retrieved 2017].
[47] "PB0051 Product Brief: RTG4 FPGAs," Rev. 1.6, Microsemi Corp., Aliso Viejo, CA, Sept. 2015, http://www.microsemi.com/document-portal/doc_view/134430-pb0051-rtg4-fpgas-product-brief [retrieved 2017].
[48] "RTG4 FPGA:DS0131Datasheet," Rev. 2i, Microsemi Corp., Aliso Viejo, CA, May 2016, http://www.microsemi.com/document-portal/doc_download/135193-ds0131-rtg4-fpga-datasheet [retrieved 2017].
[49] "SmartFusion2, IGLOO2, and RTG4L Hard Multiplier AddSub Configuration," Microsemi Corp., Aliso Viejo, CA, June 2015, http://microsemi.com/document-portal/doc_download/135182-smartfusion2-hard-multiplier-addsub-configuration-guide [retrieved 2017].
[50] "Microsemi Power Estimator: RTG4," MPE v3j, Microsemi Corp., Aliso Viejo, CA, Feb. 2016, https://www.microsemi.com/document-portal/doc_download/134921-rtg4-power-estimator [retrieved 03 July 2016].
[51] Weisstein, E. W., "Matrix Addition," *MathWorld — A Wolfram Web Resource* [online database], Jan. 2017, http://mathworld.wolfram.com/MatrixAddition.html [retrieved 01 Feb. 2017].
[52] Weisstein, E. W., "Fast Fourier Transform," *MathWorld — A Wolfram Web Resource* [online database], Jan. 2017, http://mathworld.wolfram.com/FastFourierTransform.html [retrieved 01 Feb. 2017].
[53] Weisstein, E. W., "Matrix Multiplication," *MathWorld — A Wolfram Web Resource* [online database], Jan. 2017, http://mathworld.wolfram.com/MatrixMultiplication.html [retrieved 01 Feb. 2017].
[54] Weisstein, E. W., "Convolution," *MathWorld — A Wolfram Web Resource* [online database], Jan. 2017, http://mathworld.wolfram.com/Convolution.html [retrieved 01 Feb. 2017].
[55] Weisstein, E. W., "Jacobi Transformation," *MathWorld — A Wolfram Web Resource* [online database], Jan. 2017, http://mathworld.wolfram.com/JacobiTransformation.html [retrieved 01 Feb. 2017].
[56] Weisstein, E. W., "Kronecker Product," *MathWorld — A Wolfram Web Resource* [online database], Jan. 2017, http://mathworld.wolfram.com/KroneckerProduct.html [retrieved 01 Feb. 2017].
[57] "Advance Information: PowerPC™ 603 RISC Microprocessor Technical Summary," Rev. 3, Freescale Semiconductor, Austin, TX, June 1994, http://www.nxp.com/assets/documents/data/en/data-sheets/MPC603.pdf [retrieved 2017].
[58] MPC750 RISC Microprocessor Family User's Manual, MPC750UM/D, Rev. 1, Freescale Semiconductor, Austin, TX, Dec. 2001, http://www.nxp.com/assets/documents/data/en/reference-manuals/MPC750UM.pdf.
[59] "PowerPC 740 and PowerPC7 50 Microprocessor Datasheet: Version 2.0," IBM Microelectronics Division, Hopewell Junction, NY, Sept. 2002, http://datasheets.chipdb.org/IBM/PowerPC/7xx/PowerPC-740-750.pdf [retrieved 2017].
[60] "PowerPC™ Microprocessor Family: The Bus Interface for 32-Bit Microprocessors," MPC60XBUSRM Rev. 0.1, Freescale Semiconductor, Austin, TX, Jan. 2004, http://www.nxp.com/assets/documents/data/en/reference-manuals/MPC60XBUSRM.pdf [retrieved 2017].
[61] "Tile Processor Architecture Overview for the TILEPro Series," Release 1.2, Tilera Corp. DocumentUG120, San Jose, CA, Feb. 2013, http://www.mellanox.com/repository/solutions/tile-scm/docs/UG120-Architecture-Overview-TILEPro.pdf [retrieved 2017].
[62] "Tile Processor User Architecture Manual," Release 2.4, Tilera Corp. DocumentUG101, San Jose, CA, Nov. 2011, http://www.mellanox.com/repository/solutions/tile-scm/docs/UG101-User-Architecture-Reference.pdf [retrieved 2017].
[63] "CSX700 Floating Point Processor Datasheet," 06-PD-1425 Rev. 1E, ClearSpeed Technology, Ltd., Bristol, England, U.K., Jan. 2011.
[64] "CSX600/CSX700 Instruction Set Reference Manual," 06-RM-1137 Rev. 4B, ClearSpeed Technology, Ltd., Bristol, England, U.K., Nov. 2009.
[65] Intel Quark SoC X1000 Core: Developer's Manual, Intel Corp. Order 329679-001US, Santa Clara, CA, Oct. 2013, pp. 21–23, 114, 252–290, http://www.intel.com/content/dam/support/us/en/documents/processors/quark/sb/intelquarkcore_devman_001.pdf [retrieved 2017].
[66] Intel Quark SoC X1000 Core: Hardware Reference Manual, Intel Corp. Order 329678-002US, Santa Clara, CA, April 2014, pp. 12–24, 28, http://www.intel.com/content/dam/support/us/en/documents/processors/quark/sb/329678_intelquarkcore_hwrefman_002.pdf [retrieved 2017].
[67] ARK Atom Processor Z3770 Specifications [online database], Intel Corp., Santa Clara, CA, Sept. 2013, http://ark.intel.com/products/76760 [retrieved 2017].

[68] "Intel Atom Processor Z3600 and Z3700 Series: Datasheet," Rev. 003, Intel Corp. Document 329474-003, Santa Clara, CA, Dec. 2014, http://www.intel.com/content/dam/www/public/us/en/documents/datasheets/atom-z36xxx-z37xxx-datasheet-vol-1.pdf [retrieved 2017].
[69] ARK Core i7-4610Y Processor Specifications [online database], Intel Corp., Santa Clara, CA, Sept. 2013, http://ark.intel.com/products/76618 [retrieved 2017].
[70] "Desktop 4th Generation Intel Core Processor Family, Desktop Intel Pentium Processor Family, and Desktop Intel Celeron Processor Family: Datasheet," Vol. 1, Intel Corp. Order 328897-010, Santa Clara, CA, March 2015, http://www.intel.com/content/dam/www/public/us/en/documents/datasheets/4th-gen-core-family-desktop-vol-1-datasheet.pdf [retrieved 2017].
[71] "Intel 64 and IA-32 Architectures Optimization Reference Manual," Intel Corp. Order 248966-033, Santa Clara, CA, June 2016, pp. 36–43, 62–69, http://www.intel.com/content/dam/www/public/us/en/documents/manuals/64-ia-32-architectures-optimization-manual.pdf [retrieved 2017].
[72] "Intel 64 and IA-32 Architectures Software Developer's Manual," Combined Vols. 1, 2A–2D, and 3A–3D, Intel Corp. Order 325462-060US, Santa Clara, CA, Sept. 2016, pp. 113–146, http://www.intel.com/content/dam/www/public/us/en/documents/manuals/64-ia-32-architectures-software-developer-manual-325462.pdf [retrieved 2017].
[73] Frumusanu, A., and Smith, R., "ARM A53/A57/T760 Investigated—Samsung Galaxy Note 4 Exynos Review," online publication, AnandTech, Los Angeles, CA, 10 Feb. 2015, http://www.anandtech.com/show/8718 [retrieved 2017].
[74] "ARM Cortex-A53 MPCore Processor Technical Reference Manual," DDI 0500D, Rev. r0p2, ARM Holdings, San Jose, CA, Feb. 2014, pp. 13–19, 24–29, http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0500d [retrieved 2017].
[75] "ARM Cortex-A57 MPCore Processor Technical Reference Manual," DDI 0488H, Rev. r1p3, ARM Holdings, San Jose, CA, Feb. 2016, pp. 24–27, 509–521, http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0488h [retrieved 2017].
[76] "Tile Processor and I/O Device Guide: For the TILE-Gx Family of Processors," Release 1.12, Tilera Corp. Document UG404, San Jose, CA, Oct. 2014, http://www.mellanox.com/repository/solutions/tile-scm/docs/UG404-IO-Device-Guide.pdf [retrieved 2017].
[77] "TILE-Gx Instruction Set Architecture," Release 1.2, Tilera Corp. Document UG401, San Jose, CA, Feb. 2013, http://www.mellanox.com/repository/solutions/tile-scm/docs/UG401-ISA.pdf [retrieved 2017].
[78] "Tile Processor Architecture Overview for the TILE-Gx Series," Release 1.1, Tilera Corp. Document UG130, San Jose, CA, May 2012, http://www.mellanox.com/repository/solutions/tile-scm/docs/UG130-ArchOverview-TILE-Gx.pdf [retrieved 2017].
[79] "MSC8256: Six-Core Digital Signal Processor," Freescale Semiconductor Datasheet MSC8256, Rev. 6, Austin, TX, July 2013, http://www.nxp.com/assets/documents/data/en/data-sheets/MSC8256.pdf [retrieved 2017].
[80] "MSC8256 Reference Manual: Six Core Digital Signal Processor," Rev. 0, Freescale Semiconductor Document MSC8256RM, Austin, TX, July 2011, pp. 44–72, 80–82, http://www.nxp.com/assets/documents/data/en/reference-manuals/MSC8256RM.pdf [retrieved 2017].
[81] "MSC8256 Product Brief: Six-Core DSP," Rev. 1, Freescale Semiconductor Document MSC8256PB, Austin, TX, May 2011, http://www.nxp.com/assets/documents/data/en/product-briefs/MSC8256PB.pdf [retrieved 2017]
[82] "Multicore DSP + ARM KeyStone II System-on-Chip (SoC)," Texas Instruments Document SPRS866E, Dallas, TX, Nov. 2013, http://www.ti.com/lit/ds/symlink/66ak2h12.pdf [retrieved 2017].
[83] ARM Cortex-A15 MPCore Processor Technical Reference Manual, DDI 0438I, Rev. r4p0, ARM Holdings, San Jose, CA, June 2013, pp. 12–16, 26–29, http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0438i [retrieved 2017].
[84] "ARM Architecture Reference Manual: ARMv7-A and ARMv7-R Edition," DDI 0406C.c, ARM Holdings, San Jose, CA, May 2014, pp. 165–171, 181–191, 261–272, http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0406c [retrieved 2017].
[85] "Defense-Grade Spartan-6Q Family Overview: DS172 (v1.1)," Xilinx, Inc., Product Specification, San Jose, CA, May 2014, https://www.xilinx.com/support/documentation/data_sheets/ds172_S6Q_Overview.pdf [retrieved 2017].
[86] "Xilinx Power Estimator: Extended Spartan-3A, Spartan-6," XPE 14.3, Xilinx, Inc., San Jose, CA, Oct. 2012, https://www.xilinx.com/products/technology/power/xpe/license-spartan3a.html.
[87] "Defense-Grade 7 Series FPGAs Overview: DS185 (v1.2)," Xilinx, Inc. Product Specification, San Jose, CA, July 2015, https://www.xilinx.com/support/documentation/data_sheets/ds185-7SeriesQ-Overview.pdf [retrieved 2017].
[88] "Xilinx Power Estimator: Artix-7, Kintex-7, Virtex-7, Zynq-7000," XPE 2014.1, Xilinx, Inc., San Jose, CA, April 2014, https://www.xilinx.com/products/technology/power/xpe/license-7series.html [retrieved 2017].
[89] "NVIDIA Tegra 3 HD Mobile Processors: T30 Series, AP30 Series," Technical Reference Manual DP-05644-001_v01p, NVIDIA Corp., Santa Clara, CA, Jan. 2012.
[90] "Cortex-A9 Technical Reference Manual," DDI 0388F, Rev. r2p2, ARM Holdings, San Jose, CA, April 2010, http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0388f [retrieved 2017].
[91] "NVIDIA Tegra K1: A New Era in Mobile Computing," NVIDIA Corp.Whitepaper v1.1, Santa Clara, CA, Jan. 2014, http://www.nvidia.com/content/pdf/tegra_white_papers/tegra-K1-whitepaper.pdf [retrieved 2017].
[92] "NVIDIA Tegra X1: NVIDIA's New Mobile Superchip," NVIDIA Corp.Whitepaper v1.0, Santa Clara, CA, Jan. 2015, http://international.download.nvidia.com/pdf/tegra/Tegra-X1-whitepaper-v1.0.pdf [retrieved 2017].

E. Atkins
Associate Editor