Comparative Analysis of Present and Future Space Processors with Device Metrics

CHREC
NSF Center for High-Performance Reconfigurable Computing

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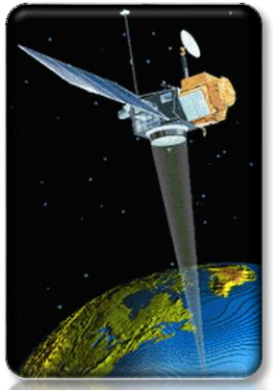
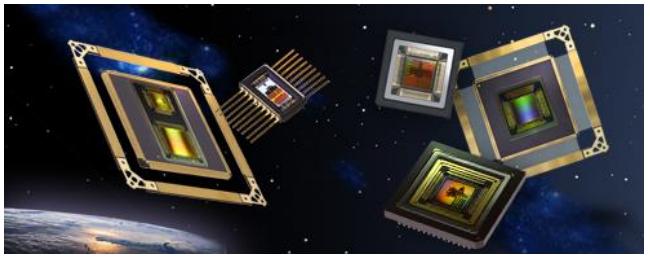
Introduction



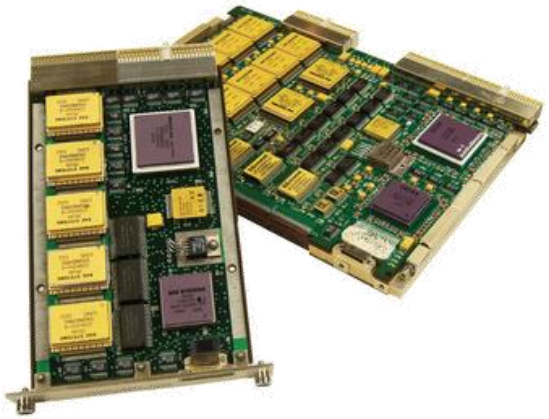
- Space computing presents unique challenges
  - Harsh and inaccessible operating environment
  - Severe resource constraints – power, size, weight
  - Stringent requirements for performance and reliability
- Increasing need for high-performance space computing
  - Escalating demands for real-time sensor and autonomous processing
  - Limited communication bandwidth to ground stations
  - Legacy space processors that cannot meet performance requirements
    - Generations behind commercial-off-the-shelf (COTS) processors
    - Based upon architectures not particularly suited to needs of space computing
- Quantitative and objective analysis of processor architectures
  - Device metrics analysis based on architectural capabilities
  - Broad and diverse set of architectures under consideration
    - Targeting space processors and low-power COTS processors (≤ 30 W)

Space Processors

- Radiation-hardened (RadHard) processors for high reliability
- Outcomes of radiation-hardening



  - Cumulative effects
    - Total-Ionizing Dose (TID) ≥ 300 krad(Si)
  - Single-Event Effects (SEEs)
    - Immunity to Single-Event Latchup (SEL), Upset (SEU), Functional Interrupt (SEFI)
  - Performance and power
    - Slower operating frequency, reduction in cores or execution units, increased power
- Techniques for radiation-hardening



  - Radiation-hardening by process
    - Insulating oxide layer used in process
  - Radiation-hardening by design
    - Specialized circuit-layout techniques
  - Radiation-hardening by architecture
    - Fault-tolerant computing strategies

Key Questions for this Study

A. How do space processors compare to one another?

B. How do space processors compare to their COTS counterparts?

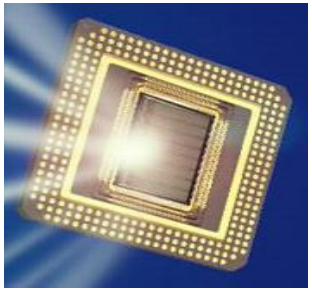
- What degree of performance overhead comes with hardening a COTS device?

C. How do top-performing COTS processors compare to one another?

D. How do top-performing COTS processors compare to top-performing space processors?

Device Metrics

- Suite of quantitative and objective metrics developed by NSF CHREC Center at University of Florida [1-2]
  - For comparative analysis of broad and diverse set of processors
    - Central processing units (CPUs)
    - Digital signal processors (DSPs)
    - Field-programmable gate arrays (FPGAs)
    - Graphics processing units (GPUs)
    - Hybrid combinations of above (often SoCs)



  - Highly useful for first-order analyses and comparisons
    - Study broad range of devices with metrics to determine best candidates
    - Later, study best candidates more deeply with selected, optimized benchmarking
  - Different methods used for fixed- and reconfigurable-logic devices
- Metrics data collected from architectural features of device
  - Determined from vendor-provided information and tools
    - Experimental testbed in lab is not required for metrics analysis

[1] J. Williams, A. George, J. Richardson, K. Gosrani, C. Massie, H. Lam, "Characterization of Fixed and Reconfigurable Multi-Core Devices for Application Acceleration," ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 3, No. 4, Nov. 2010, pp. 19:1-19:29.

[2] J. Richardson, S. Fingulin, D. Raghunathan, C. Massie, A. George, and H. Lam, "Comparative Analysis of HPC and Accelerator Devices: Computation, Memory, I/O, and Power," Proc. of High-Performance Reconfigurable Computing Technology and Applications Workshop (HPRCTA), at SC'10, New Orleans, LA, Nov 14, 2010.

Device Metrics Analysis

- Analyzing performance (GOPS) and power (GOPS/W)
  - Computational Density (**CD**) measures theoretical performance
    - Reported in giga-operations per second (GOPS)
    - Calculated separately for varying data types
      - 8-bit, 16-bit, and 32-bit Integer (Int8, Int16, and Int32)
      - Single-precision and double-precision floating point (SPFP and DPFP)
    - Determine operations mix (additions, multiplications, etc.) based on target apps
  - CD per Watt (**CD/W**) measures performance scaled by power
- Analyzing memory and input-output bandwidth (GB/s)
  - Internal Memory Bandwidth (**IMB**) measures throughput between processor and on-chip memory (cache or BRAM)
  - External Memory Bandwidth (**EMB**) measures throughput between processor and off-chip memory (DDR2, DDR3, etc)
  - Input-Output Bandwidth (**IOB**) measures throughput between processor and all off-chip resources (DDR, GigE, PCIe, GPIO, etc.)

Device Metrics: CPU Analysis (1/2)

- **Example: Freescale P5040**
  - COTS counterpart of RadHard RAD5545 CPU from BAE Systems
  - Fixed-logic CPU: 2.2 GHz, 49 W, quad-core, no SIMD engine
- Calculating CD and CD/W
  - Each core contains
    - 3 integer execution units 1 floating-point execution unit
      - Can issue 2 instructions each cycle
  - Calculate operations/cycle for each data type
    - Int8: 2 ops/cycle Int16: 2 ops/cycle Int32: 2 ops/cycle
    - SPFP: 1 op/cycle DPFP: 1 op/cycle

Operations mix of 50% add, 50% mult

- $CD_{Int8,Int16,Int32}$ = 4 cores × 2.2 GHz × 2 ops/cycle = **17.6 GOPS**
- $CD/W_{Int8,Int16,Int32}$ = 17.6 GOPS / 49 W = **0.36 GOPS/W**
- $CD_{SPFP,DPFP}$ = 4 cores × 2.2 GHz × 1 ops/cycle = **8.8 GOPS**
- $CD/W_{SPFP,DPFP}$ = 8.8 GOPS / 49 W = **0.18 GOPS/W**

Device Metrics: CPU Analysis (2/2)

- Calculating IMB, EMB, and IOB
  - Each core contains
    - L1 data cache: 8-byte bus L1 instr cache: 16-byte bus L2 cache: 64-byte bus
  - Total of 2 DDR3 controllers: 8-byte bus; 1600 MT/s
  - IMB_{L1data} = 4 cores × 2.2 GHz × 8 bytes = **70.4 GB/s**
  - IMB_{L1inst} = 4 cores × 2.2 GHz × 16 bytes = **140.8 GB/s**
  - IMB_{L2} = 4 cores × 2.2 GHz × 64 bytes = **563.2 GB/s**
  - EMB = 2 DDR3 × 8 bytes × 1600 MT/s = **25.6 GB/s**
  - IOB = DDR3 + 10GigE + 1GigE + PCIe + SATA2.0 + GPIO
    = 25.6 GB/s + 5 GB/s + .5 GB/s
    + 8 GB/s + .3 GB/s + 8.8GB/s = **48.2 GB/s**

Assumes 100% cache hit rate

Based on optimal SerDes lane config.

Device Metrics: FPGA Analysis (1/2)

- **Example: Xilinx Virtex-5 FX130T**
  - COTS counterpart of RadHard Virtex-5QV FX130 FPGA from Xilinx
  - Reconfigurable-logic FPGA: different methods required for metrics [3]
- Calculating CD and CD/W
  - FPGA logic resources
    - Look-up tables (LUTs), Flip-flops (FFs), Multiply-accumulate units (DSPs)
  - Generate and implement compute cores on FPGA with vendor tools
    - All combinations of operation and data types: with and without DSP resources
    - Collect data on resource usage and max. operating frequencies
    - Linear-programming algorithm optimally packs cores onto FPGA
    - Max. cores = max. ops/cycle (with pipelined cores)
  - Use vendor-provided tools for power estimation
    - Calculate dynamic power based on resource usage for cores
  - CD_{Int8} = 2358 ops/cycle × 0.353 GHz = **833.2 GOPS**
  - CD/W_{Int8} = 833.2 GOPS / 15.87 W = **52.5 GOPS/W**

Operations mix of 50% add, 50% mult

Same process used for all data types

[3] N. Wulf, J. Richardson, and A. George, "Optimizing FPGA Performance, Power, and Dependability with Linear Programming," Proc. of Military and Aerospace Programmable-Logic Devices Conference (MAPLD), San Diego, CA, April 9 - 12, 2013.

Device Metrics: FPGA Analysis (2/2)

- Calculating IMB, EMB, and IOB
  - 298 Block RAM units (BRAMs): 9-byte bus, 2 ports, 0.450 GHz operating frequency
  - 5 DDR2 controllers: 8-byte bus, double data rate, 0.266 GHz operating frequency
  - 840 GPIO pins: 0.8 Gb/s data rate
  - 20 RocketIO GTX transceivers: 6.5 Gb/s data rate

Based on max. packing of memory controllers

  - IMB_{BRAM} = 298 BRAMs × 0.450 GHz × 9 bytes × 2 ports = **2413.8 GB/s**
  - EMB = 5 DDR2 × 0.266 GHz × 8 bytes × 2 (double data rate) = **21.33 GB/s**
  - IOB = DDR2 + GPIO + RocketIO GTX transceivers
    = 21.33 GB/s + (840 pins × 0.8 Gb/s)
    + (20 transceivers × 6.5 Gb/s) = **121.58 GB/s**

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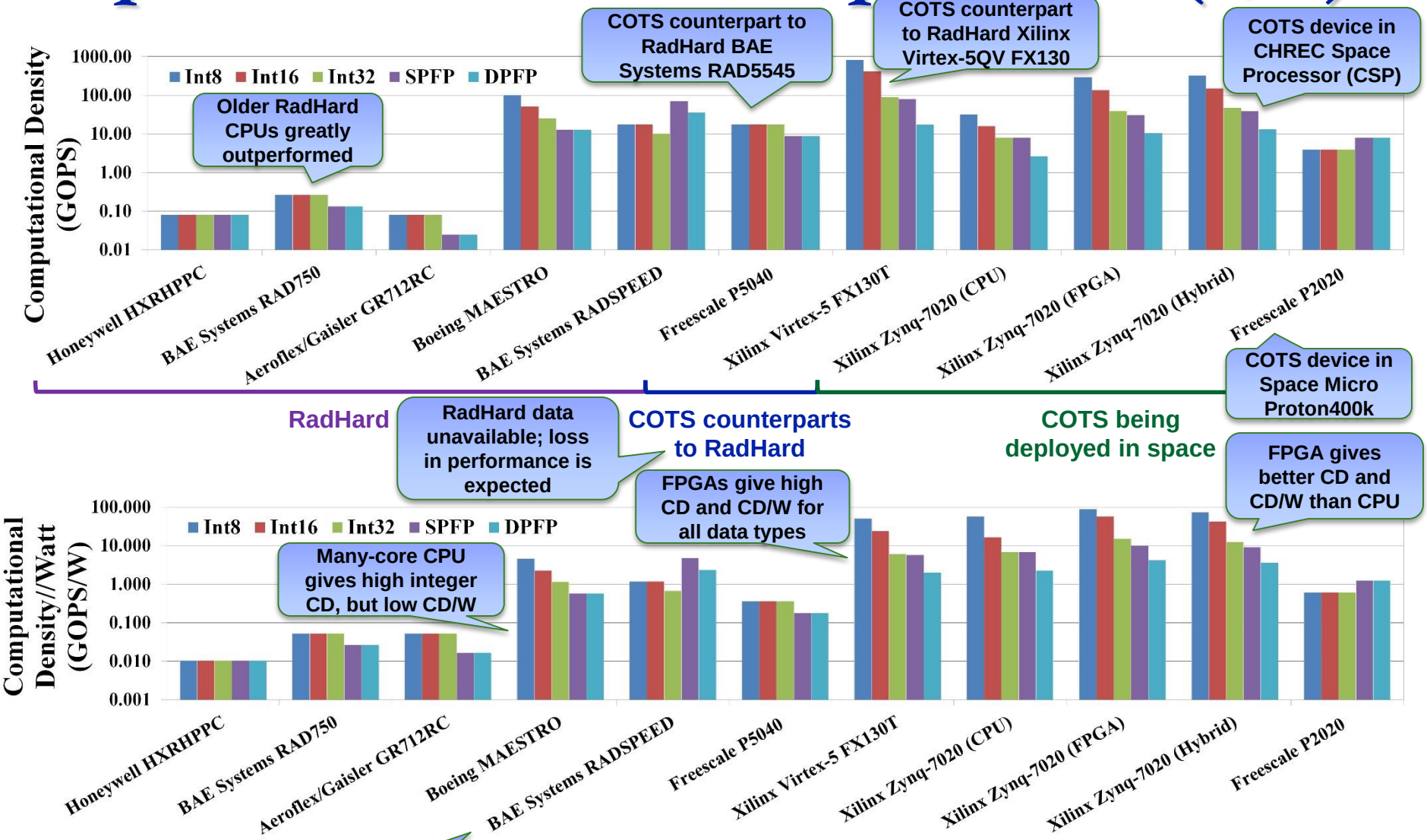
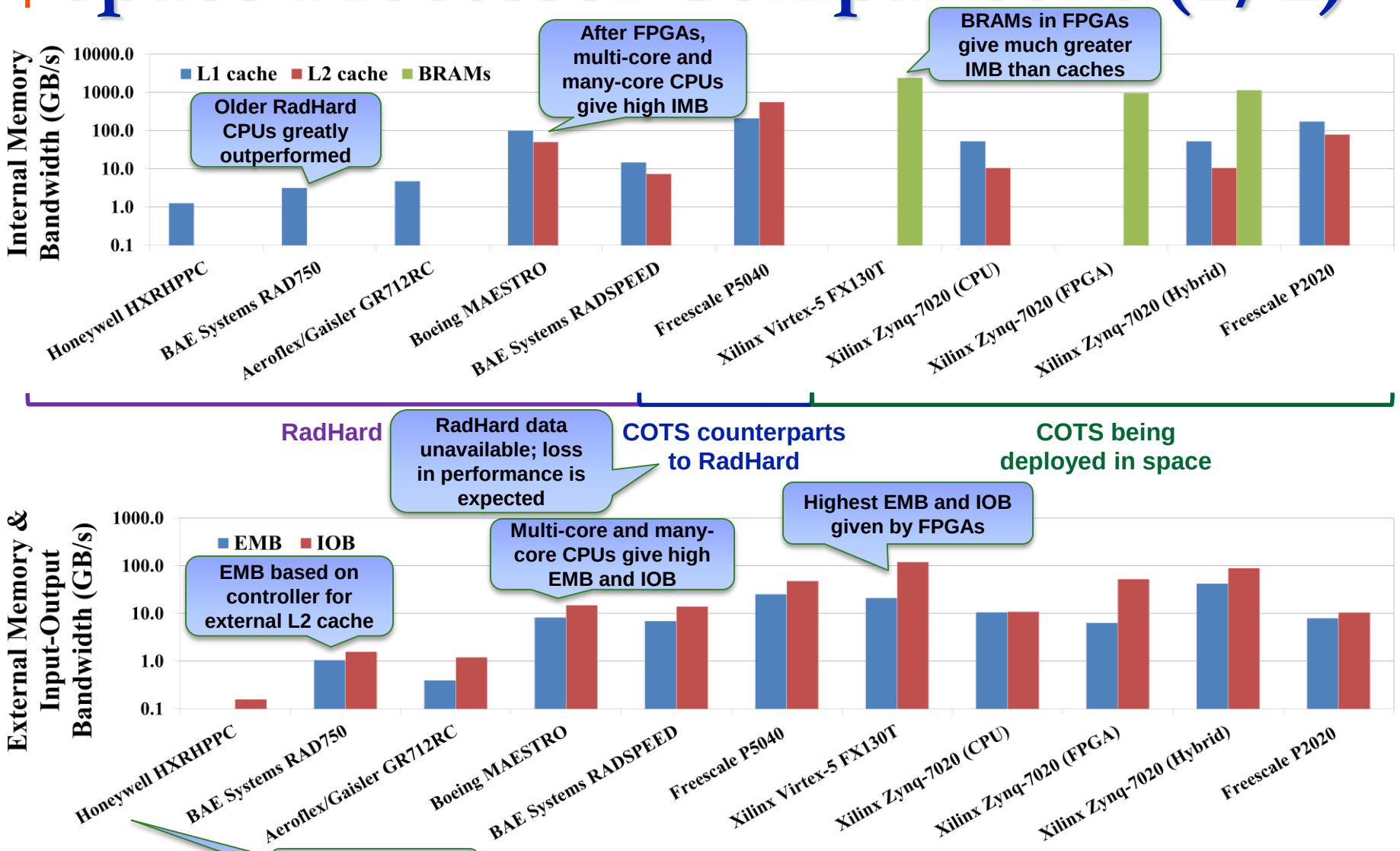
Space Processor Comparisons (1/2)



Results displayed in logarithmic scale

Space Processor Comparisons (2/2)



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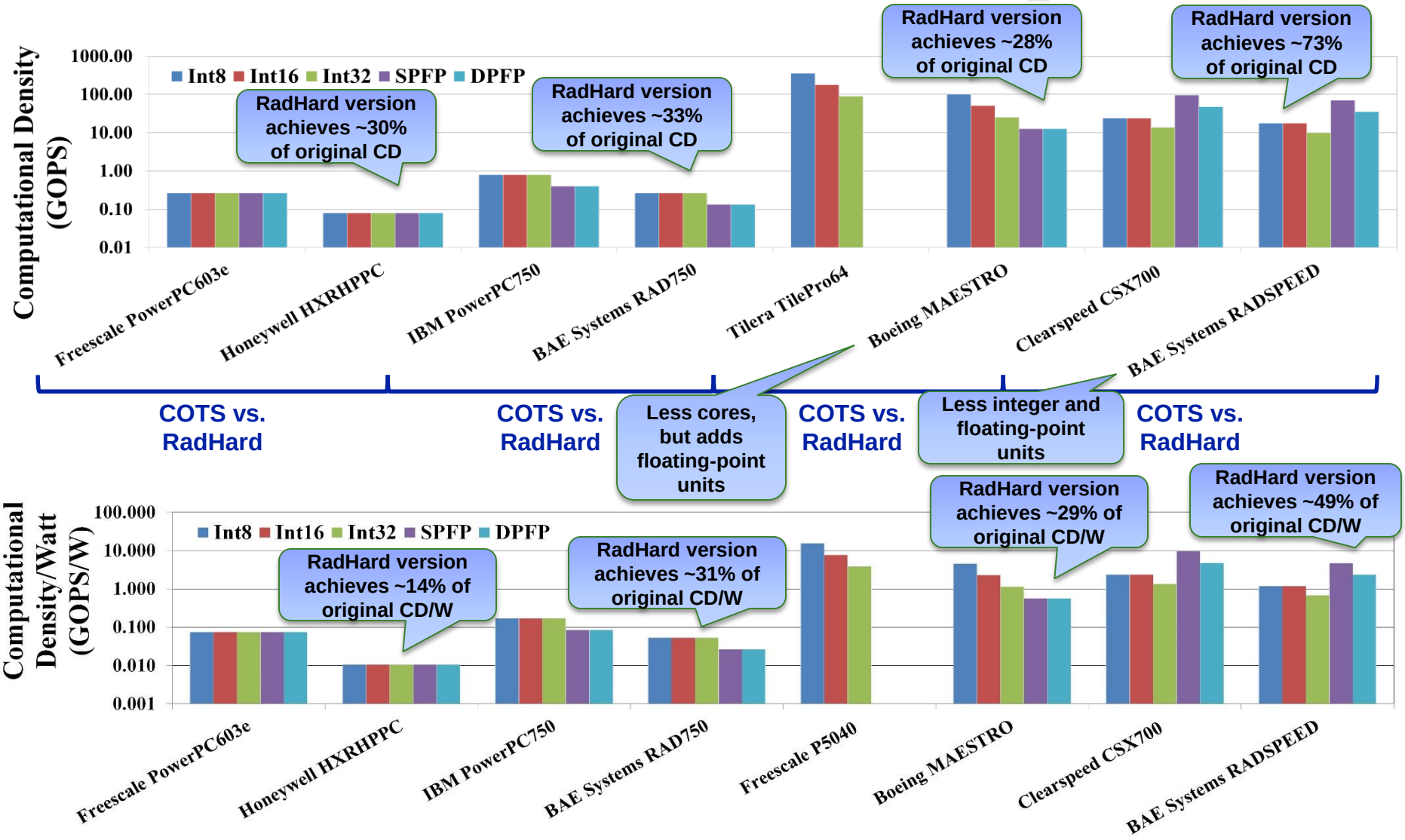
RadHard vs. COTS Counterparts (1/2)



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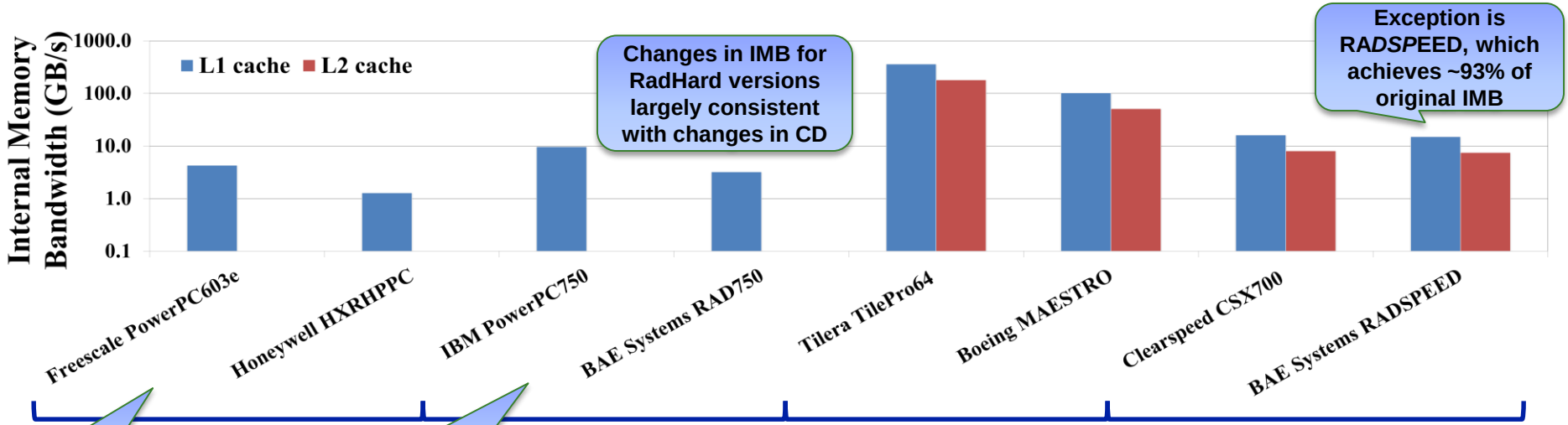
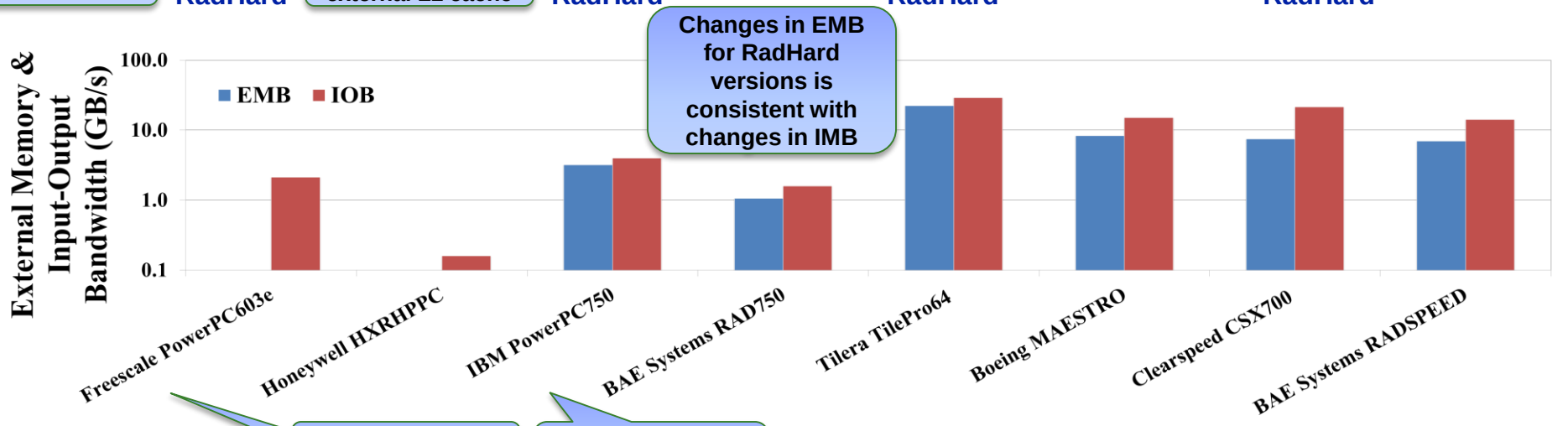
RadHard vs. COTS Counterparts (2/2)





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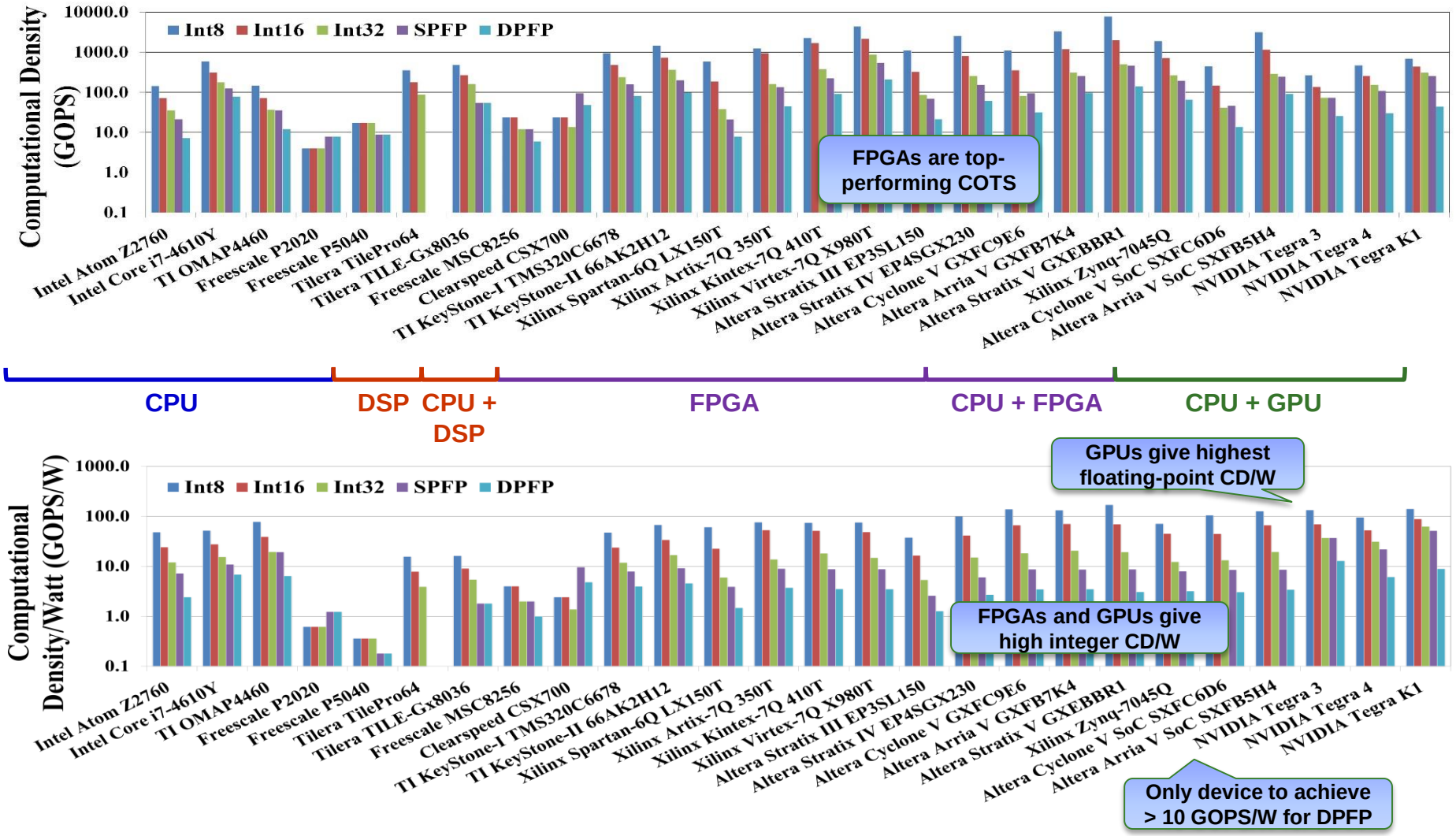

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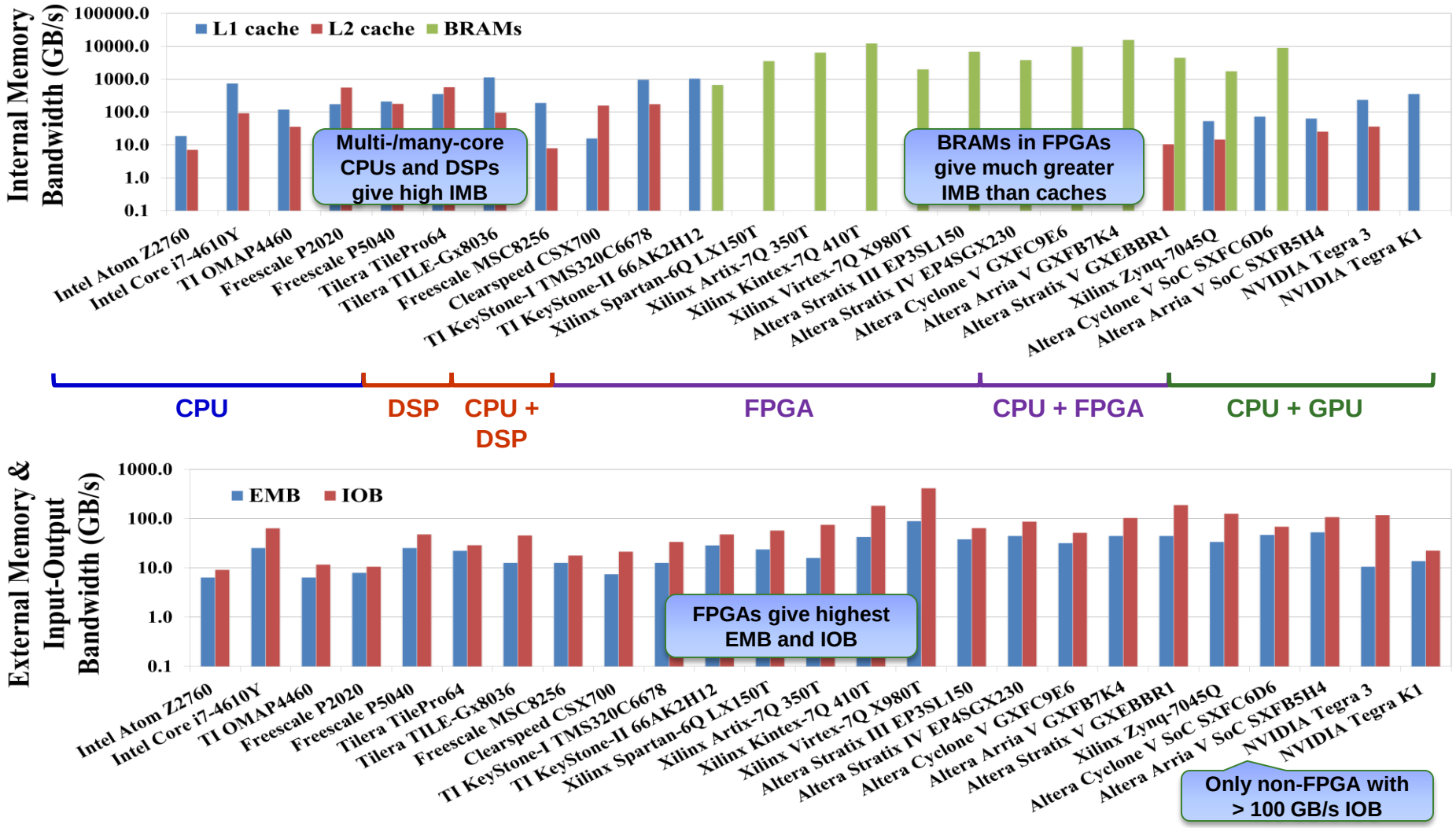
COTS Processor Comparisons (2/2)



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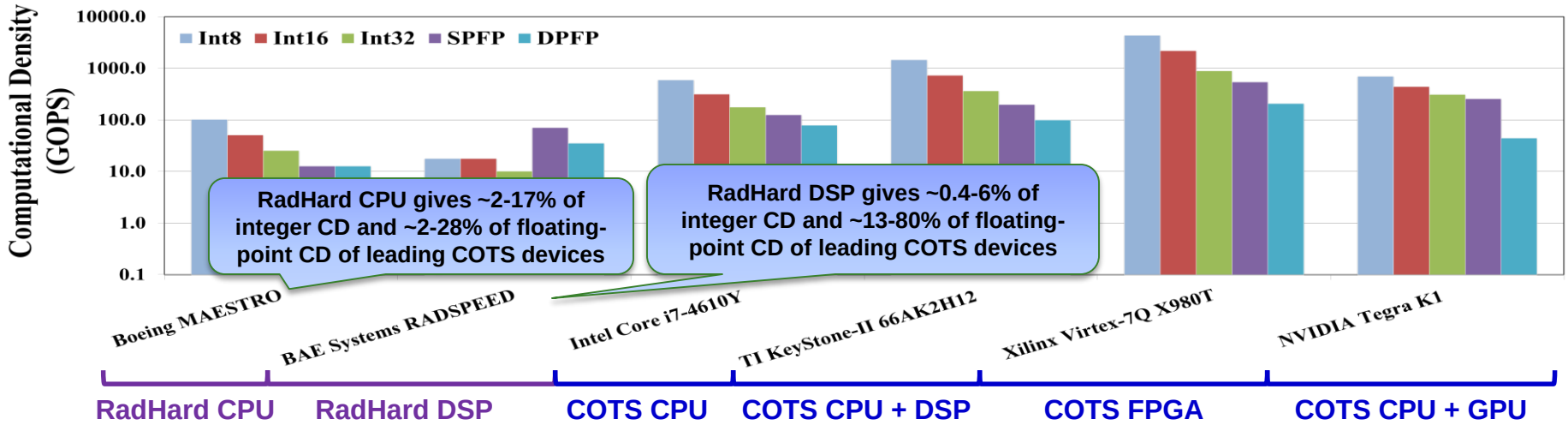

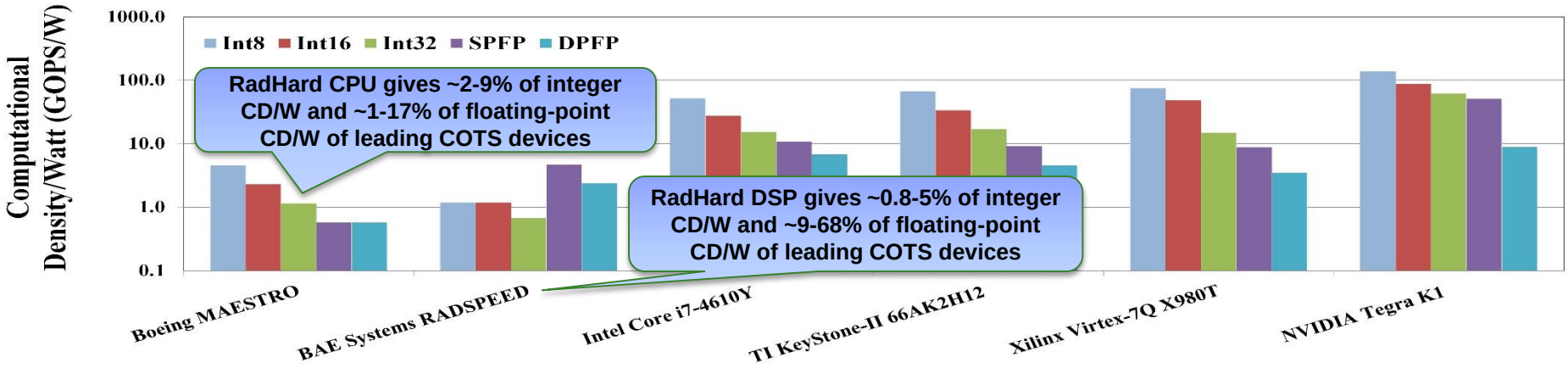

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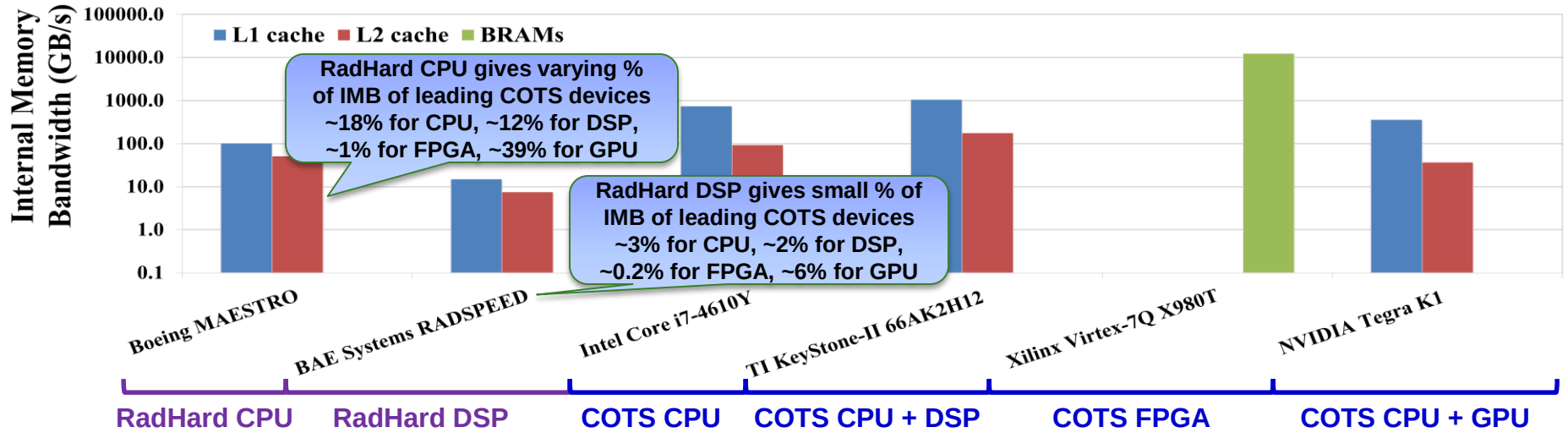
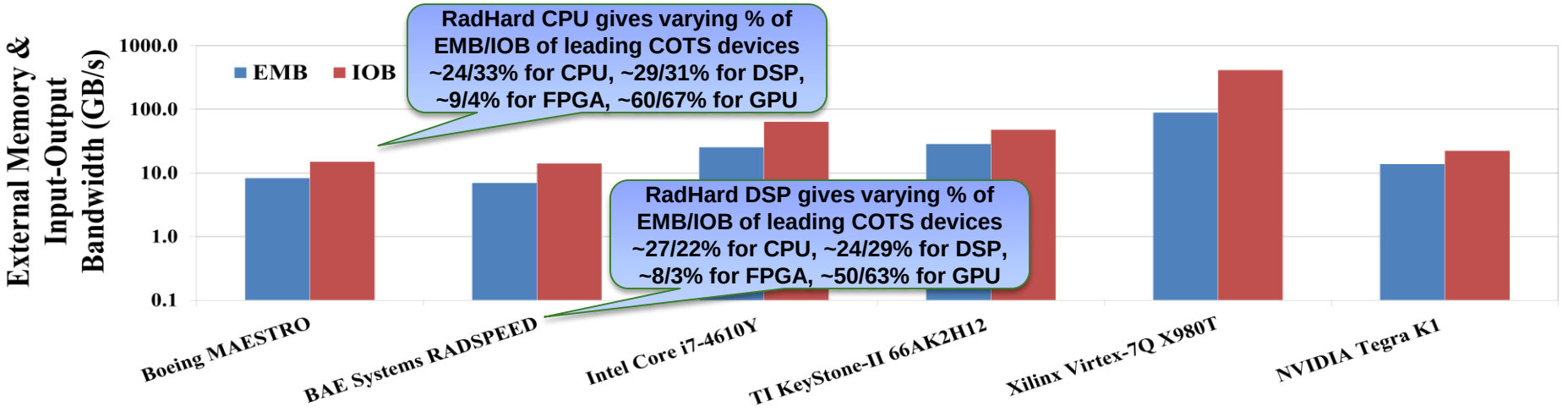
RadHard vs. COTS Comparisons (2/2)





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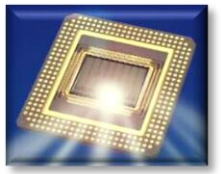
Conclusions and Future Research

- Comparative analysis of present and future space processors
  - Broad and diverse set of architectures under consideration
    - Targeting space processors and low-power COTS processors (≤ 30 W)
    - Multi-core and many-core CPUs, DSPs, FPGAs, GPUs, and Hybrid combinations
  - Quantitative analysis with device metrics (CD, CD/W, IMB, EMB, IOB)
    - Two top-performing RadHard processors observed in this study
      - RadHard DSP (floating-point) and RadHard many-core CPU (integer)
    - RadHard processors achieve ~**28**-**33**% of original COTS performance (CD)
      - Exception is RadHard DSP with ~**73**% of original COTS performance
    - FPGAs are top-performing COTS processors, but GPUs compete in CD/W
    - Hardening of top COTS would raise available RadHard performance in most cases
      - RadHard CPU gets ~**2**-**17**% in integer CD and ~**2**-**28**% in float CD of top COTS devices
      - RadHard DSP gets ~**0.4**-**6**% in integer CD and ~**13**-**80**% in float CD of top COTS devices

- Next step? Expand results with additional processors
  - More RadHard devices as info attained (e.g., RAD5545, V5QV)
    - As well as new combinations (e.g., RAD5545+RA*DSP*EED)
  - Best COTS devices with potential for hardening & use in space



Appendix: Device Metrics Data

	Processor	Type	CD (GOPS)					CD/W (GOPS/W)					IMB (GB/s)			EMB (GB/s)	IOB (GB/s)
			Int8	Int16	Int32	SPFP	DPFP	Int8	Int16	Int32	SPFP	DPFP	L1 cache	L2 cache	BRAMs		
RadHard	Honeywell HXRHPPC	CPU	0.080	0.080	0.080	0.080	0.080	0.011	0.011	0.011	0.011	0.011	1.280	0.000	0.000	0.000	0.160
	BAE Systems RAD750	CPU	0.266	0.266	0.266	0.133	0.133	0.053	0.053	0.053	0.027	0.027	3.192	0.000	0.000	1.064	1.592
	Aeroflex/Gaisler GR712RC	CPU	0.080	0.080	0.080	0.025	0.025	0.053	0.053	0.053	0.017	0.017	4.800	0.000	0.000	0.400	1.213
	Boeing MAESTRO	CPU	101.920	50.960	25.480	12.740	12.740	4.591	2.295	1.148	0.574	0.574	101.920	50.960	0.000	8.320	15.070
	BAE Systems RADSPEED	DSP	17.708	17.708	10.119	70.832	35.416	1.181	1.181	0.675	4.722	2.361	14.912	7.456	0.000	6.990	14.185
COTS counterparts to RadHard	Freescale PowerPC603e	CPU	0.266	0.266	0.266	0.266	0.266	0.076	0.076	0.076	0.076	0.076	4.256	0.000	0.000	0.000	2.128
	IBM PowerPC750	CPU	0.800	0.800	0.800	0.400	0.400	0.170	0.170	0.170	0.085	0.085	9.600	0.000	0.000	3.200	4.000
	Tilera TilePro64	CPU	358.400	179.200	89.600	0.000	0.000	15.583	7.791	3.896	0.000	0.000	358.400	179.200	0.000	22.400	29.150
	Freescale P5040	CPU	17.600	17.600	17.600	8.800	8.800	0.359	0.359	0.359	0.180	0.180	211.200	563.200	0.000	25.600	48.200
	Clearspeed CSX700	DSP	24.000	24.000	13.714	96.000	48.000	2.400	2.400	1.371	9.600	4.800	16.000	8.000	0.000	7.500	21.500
	Xilinx Virtex-5 FX130T	FPGA	833.200	416.300	89.680	80.230	17.530	52.500	24.740	6.372	6.038	2.191	0.000	0.000	2413.800	21.334	121.584
COTS being deployed in space	Freescale P2020	CPU	4.000	4.000	4.000	8.000	8.000	0.615	0.615	0.615	1.231	1.231	176.000	80.000	0.000	8.000	10.620
	Xilinx Zynq-7020 (CPU)	CPU	32.020	16.010	8.000	8.000	2.670	57.610	16.720	6.860	6.860	2.290	53.360	10.670	0.000	10.664	11.030
	Xilinx Zynq-7020 (FPGA)	FPGA	292.130	135.990	39.340	30.740	10.460	88.260	57.140	15.130	10.060	4.210	0.000	0.000	978.264	6.400	53.050
	Xilinx Zynq-7020 (Hybrid)	CPU+FPGA	324.150	152.000	47.340	38.740	13.130	72.350	42.820	12.560	9.160	3.590	53.360	10.670	978.264	42.656	89.670
COTS	Intel Atom Z2760	CPU	144.000	72.000	36.000	21.600	7.200	48.000	24.000	12.000	7.200	2.400	18.800	7.200	0.000	6.400	9.192
	Intel Core i7-4610Y	CPU	594.600	316.200	177.000	124.800	78.400	51.704	27.496	15.391	10.852	6.817	742.400	92.800	0.000	25.600	64.100
	TI OMAP4460	CPU	146.170	73.090	36.540	36.140	12.000	77.420	38.710	19.360	19.140	6.360	120.000	36.000	0.000	6.400	11.710
	Tilera TILE-Gx8036	CPU	486.000	270.000	162.000	54.000	54.000	16.200	9.000	5.400	1.800	1.800	1152.000	576.000	0.000	12.800	45.920
	Freescale MSC8256	DSP	24.000	24.000	12.000	12.000	6.000	3.974	3.974	1.987	1.987	0.993	192.000	96.000	0.000	12.800	17.940
	TI KeyStone-I TMS320C6678	DSP	960.000	480.000	240.000	160.000	80.000	47.291	23.645	11.823	7.880	3.940	960.000	160.000	0.000	12.800	33.860
	TI KeyStone-II 66AK2H12	CPU+DSP	1459.200	729.600	364.800	198.400	99.200	67.280	33.640	16.820	9.150	4.570	1049.600	176.000	0.000	28.800	48.220
	Xilinx Spartan-6Q LX150T	FPGA	590.400	185.100	37.960	21.220	7.859	60.580	22.460	5.947	3.889	1.467	0.000	0.000	675.360	24.000	57.800
	Xilinx Artix-7Q 350T	FPGA	1245.000	939.100	163.300	134.200	45.520	75.490	52.650	13.730	8.930	3.721	0.000	0.000	3598.614	16.000	75.600
	Xilinx Kintex-7Q 410T	FPGA	2295.000	1696.000	380.600	224.300	91.950	74.280	51.360	18.030	8.715	3.500	0.000	0.000	6555.268	42.667	184.292
	Xilinx Virtex-7Q X980T	FPGA	4356.000	2186.000	890.500	539.600	207.200	75.230	48.310	14.790	8.764	3.469	0.000	0.000	12368.430	89.600	417.425
	Altera Stratix III EP3SL150	FPGA	1115.000	329.700	87.100	69.430	21.550	37.470	16.460	5.332	2.575	1.264	0.000	0.000	2020.140	38.400	64.800
	Altera Stratix IV EP4SGX230	FPGA	2563.000	811.500	258.100	153.000	60.550	99.320	41.230	15.040	5.995	2.694	0.000	0.000	6906.600	44.800	87.900
	Altera Cyclone V GXFC9E6	FPGA	1113.000	358.800	81.530	94.170	31.810	138.300	65.970	18.170	8.645	3.463	0.000	0.000	3843.000	32.000	51.813
	Altera Arria V GXFB7K4	FPGA	3329.000	1197.000	310.000	260.700	97.100	131.800	70.330	20.610	8.607	3.481	0.000	0.000	9656.000	44.800	103.800
	Altera Stratix V GXEBBR1	FPGA	7885.000	1999.000	499.000	461.300	140.600	168.900	69.100	19.230	8.669	3.063	0.000	0.000	15840.000	44.800	191.125
	Xilinx Zynq-7045Q	CPU+FPGA	1896.020	719.810	269.200	194.100	65.270	70.640	44.690	12.250	7.930	3.170	53.360	10.670	4493.863	34.110	126.630
	Altera Cyclone V SoC SXFC6D6	CPU+FPGA	454.800	149.500	40.990	45.960	13.840	104.480	44.560	13.230	8.510	3.030	74.000	14.800	1754.550	46.930	69.180
	Altera Arria V SoC SXFB5H4	CPU+FPGA	3168.400	1170.200	294.200	246.900	91.290	125.680	65.960	19.300	8.520	3.400	64.000	0.000	9128.000	53.330	107.960
	NVIDIA Tegra 3	CPU+GPU	265.984	137.984	73.984	73.984	25.600	132.992	68.992	36.992	36.992	12.800	240.000	25.600	0.000	10.680	118.400
	NVIDIA Tegra 4	CPU+GPU	473.980	261.180	154.780	109.180	30.400	94.800	52.240	30.960	21.840	6.080	--	--	0.000	--	--
	NVIDIA Tegra K1	CPU+GPU	697.600	440.000	311.200	256.000	44.400	139.520	88.000	62.240	51.200	8.880	358.400	36.800	0.000	13.854	22.550