INVITED PAPER

Onboard Processing With Hybrid and Reconfigurable Computing on Small Satellites

This paper surveys the challenges and opportunities of onboard computers for small satellites and focuses upon new concepts, methods, and technologies that are revolutionizing their capabilities, in terms of two guiding themes: hybrid computing and reconfigurable computing.

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ABSTRACT | Due to the increasing demands of onboard sensor and autonomous processing, one of the principal needs and challenges for future spacecraft is onboard computing. Space computers must provide high performance and reliability (which are often at odds), using limited resources (power, size, weight, and cost), in an extremely harsh environment (due to radiation, temperature, vacuum, and vibration). As spacecraft shrink in size, while assuming a growing role for science and defense missions, the challenges for space computing become particularly acute. For example, processing capabilities on CubeSats (smaller class of SmallSats) have been extremely limited to date, often featuring microcontrollers with performance and reliability barely sufficient to operate the vehicle let alone support various sensor and autonomous applications. This article surveys the challenges and opportunities of onboard computers for small satellites (SmallSats) and focuses upon new concepts, methods, and technologies that are revolutionizing their capabilities, in terms of two guiding themes: hybrid computing and reconfigurable computing. These innovations are of particular need and value to CubeSats and other SmallSats. With new technologies, such as CHREC Space Processor (CSP), we demonstrate how system designers can exploit hybrid and reconfigurable computing on SmallSats to harness these advantages for a variety of purposes, and we highlight several recent missions by NASA and industry that feature these principles and technologies.

KEYWORDS | Fault-tolerant systems; field-programmable gate arrays; radiation effects; reconfigurable architectures; satellites; space radiation

I. INTRODUCTION

The landscape of spacecraft development and space-mission concepts are in the midst of a dramatic paradigm shift, stemming from novel advances in technology and compelling, successful demonstrations of small-spacecraft missions. This fundamental change is moving toward small-satellite (SmallSat) missions and shifting away from traditionally large, monolithic satellites. The growing importance of SmallSat missions has been gestating as a future outcome from as early as 2000, as described by the National Research Council's (NRC) publication "The Role of Small Satellites in NASA and NOAA Earth Observation Programs," and has been now burgeoning in recent years [1]. The rationale dictated in this study for the advancement of SmallSats largely remains unchanged to date. The study stressed the benefits of SmallSats, as low-cost yet capable platforms offering great architectural and programmatic flexibility. Additionally, the study highlighted unique design features that apply to SmallSats, such as distributed functions, observation strategies (constellations and clusters), rapid infusion of technology, and both budget and schedule flexibility. SmallSats, especially in the range of nanosatellites and microsatellites, have

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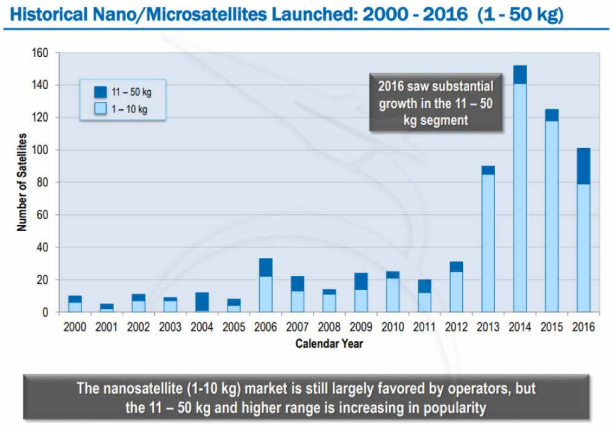

Fig. 1. ***SpaceWorks historical nano/microsatellite launches [3].***

rapidly become more advanced and have been featured in more missions in recent years. This growth has been attributed to CubeSat (sub-class of SmallSat) research programs started by the National Science Foundation (NSF), which has incited university participation and a growing commercial interest from industry for using SmallSats in Earth observations and remote sensing [2]. Correspondingly, the number of CubeSat launches has rapidly expanded. SpaceWorks, a company that focuses on monitoring global satellite activities, publishes studies on its findings annually [3]. In Fig. 1, SpaceWorks highlights a sudden increase in SmallSats in the 1–50-kg range from 2000 until 2016, emphasizing major changes in the space development ecosystem.

In 2015, the National Aeronautics and Space Administration (NASA) released a technology roadmap to describe the future development efforts required to create novel, cutting-edge technologies that enable new capabilities for ambitious future space missions [4]. In this roadmap, there are 15 distinct technology areas (launch propulsion systems, science, instruments, observatories, sensor systems, etc.) relating to different aspects that comprise space missions. Additionally, they note technology topics that encompass and overlap multiple areas. One of these domain-crossing technology topics is avionics, which focuses on the electronic systems that are essential to satellite capabilities.

In 2016, the NRC published a study [5] that investigated all the topics found in the roadmap to provide recommendations of focus for NASA, ranking the topics in order of importance, and classifying key topics as "high-priority." Eight eight topics were classified as high-priority technologies, and 26 of those 88 (roughly 30%) are encapsulated by avionics, further highlighting the significance of computing and processing for space operations. SmallSats can play a crucial role in advancing key technology roadmap topics through technology demonstration of new computers and systems.

Even though the most popular space platform (CubeSats) is small, the demands for advanced science and capabilities are always increasing. Both future missions and spacecraft have a principal need for high performance and reliability. Therefore, the major challenge developing future spacecraft is to balance the demands of onboard sensor and science processing with the limitations of reduced power, size, weight, and cost of a SmallSat platform. Current SmallSat computing technologies, especially devices found in CubeSats, are prohibitively limited, often featuring microcontrollers which scarcely approach the processing or reliability requirements for extensive science objectives. Even SmallSats equipped with more high-performance, modern processors meeting performance needs, may face reliability concerns due to hazardous radiation in space environments. SmallSat missions do not amass the funding of larger spacecraft missions, therefore purchasing state-of-the-art, radiation-hardened (rad-hard) processors is often infeasible, due to extremely high costs. Additionally, while rad-hard processors may meet reliability needs, a state-of-the-art, rad-hard processor is relatively antiquated in terms of energy efficiency and performance compared to most modern commercial processors. Therefore, rad-hard processors are unable to achieve the computing capability needed for high-priority tasks in the technology roadmap, especially for compute-intensive autonomous operations and complex sensor processing. Illustrating the need for reliable computers meeting mission needs, in his 2015 keynote address [6] to the (AIAA) Small Satellite Conference, General John Hyten, former Commander of the Air Force Space Command, noted:

> We need to build computers with resilient architectures that meet operational and mission requirements and logistically support a continued supply chain.

This paper presents a survey of the challenges and opportunities of onboard computers for small satellites (SmallSats) and focuses upon new concepts, methods, and technologies, to provide next-generation missions with the performance and reliability required to meet their objectives. There are two guiding themes driving revolutionary capabilities of SmallSat computing, namely, hybrid computing and reconfigurable computing. We define reconfigurable computing as a set of architecture and programming methodologies with which reconfigurable logic can be customized to meet the unique needs of each application, thereby achieving greater performance and versatility with less resources. We define hybrid computing as a mix of dissimilar computing technologies to gain their collective advantages, such as a combination of rad-hard devices with commercial devices to achieve both high reliability and performance. These innovations are critical to meeting future science and defense technology goals. This paper then highlights new technologies, such as the CHREC Space Processor (CSP), where we demonstrate how system designers can exploit hybrid and reconfigurable computing on SmallSats to harness these advantages for a variety of purposes. Finally, we highlight recent missions by NASA and industry that feature these principles and technologies.

II. BACKGROUND

This section provides a cursory overview of the effects of space radiation on electronics. Additionally, this section further defines the scope and concepts of reconfigurable and hybrid architecture, as well as fault-tolerant computing techniques applied to those designs. Finally, more detailed information is provided on SmallSats with an emphasis on the CubeSat subset.

A. Radiation Effects on Electronics

The principal challenge for sustained, reliable computing in space arises from the environmental hazards of radiation to electrical, electronic, and electromechanical (EEE) parts. EEE parts in space can be exposed to a wide range of radiation environments, each with considerably different types of particles and fluences, which lead to varying responses from negligible degradation or benign interrupt to complete and catastrophic failure. There is no generalized or common-case space environment; therefore, radiation effects must be analyzed on a per-mission basis.

Particles encountered in space can originate from several sources including Earth's magnetic field, galactic cosmic rays (GCRs), and solar-weather events. Earth's magnetic field primarily consists of low-energy charged particles (electrons and protons) and some heavy ions. GCRs originate from outside the solar system and are primarily protons and alpha particles, however, heavy ions are also present in comparably low numbers. Finally, solar-weather events consist of solar winds, solar flares, and coronal mass ejections (CMEs), which are predominately protons and a small fraction of heavy ions.

When these particles interact with electronic components, the effects can be generally classified into two categories: long-term cumulative effects and short-term transient effects (commonly described as single-event effects). Cumulative effects include a buildup of total ionizing dose (TID) levels, ionization of circuits, enhanced low-dose-rate sensitivity (ELDRS), and displacement-damage dose (DDD). The single-event effects (SEEs) category includes single-event upsets (SEUs), single-event transients (SETs), single-event latchups (SELs), single-event burnouts (SEBs), single-event functional interrupts (SEFIs), and last, single-event gate ruptures (SEGRs). EEE components (even an identical device from a different lot) can react differently to radiation, and experience different effects more prominently. Radiation-effect testing is a broad field with extensive studies on the complex relationship of various devices (including processors) to radiation. Space environment and radiation effects are further covered in [7]–[10].

To examine the effectiveness of electronic technologies in space environments, NASA has a dedicated agency-wide program called the NASA Electronic Parts and Packaging (NEPP) program [11]. NEPP performs several functions to assist organizational programs and missions including guidance to missions for electronic part selection, resources to understand risks related to components, evaluations for NASA mission assurance, and finally guidelines and documents for testing. NEPP encapsulates the following activities: EEE parts reliability, radiation assurance, EEE radiation effects, EEE parts packaging, and EEE parts assurance. A key topic covered by the program includes radiation hardness assurance (RHA) for flight programs, which is a NASA-recommended approach to designing reliable space systems [12]. NEPP has also collected a series of examples in [13] that describes spacecraft anomalies during solar events, including spontaneous processor resets, memory errors, and instrument failures.

B. Reconfigurable Computing

Reconfigurable computing is a subset of computer architecture that focuses upon devices with adaptive designs that can be programmed to create different architectures and circuits. The devices most commonly associated with reconfigurable computing are field-programmable gate arrays (FPGAs). There are several advantages of using an FPGA over a general-purpose CPU or microprocessor. First, FPGAs enable a designer to create custom, application-specific architectures to exploit algorithmic parallelism. Also, FPGAs are typically more energy efficient than a general-purpose processor, enabling a designer to achieve massive computational speedup on an application while consuming less energy. In addition, due to the flexible, reconfigurable design of the architecture, FPGAs are frequently employed to interface multiple high-bandwidth sensors to a system (commonly referred to as "interface glue logic"), since designers can configure the input/output pins as needed.

FPGAs are desirable for use in space because many space applications, such as synthetic aperture radar (SAR), hyperspectral imaging (HSI), image processing, and image compression, are highly amenable to parallelization within an FPGA. This approach enables missions to perform critical data processing onboard, which can preserve transmission bandwidth, as opposed to transmitting an entire data set for processing on the ground. Additionally, some FPGAs support more flexibly with runtime reconfiguration of sections of the architecture with a feature known as partial reconfiguration.

Unfortunately, while more powerful, commercial SRAM-based FPGAs are sensitive to radiation in space. FPGAs are highly reconfigurable, and rely on their configuration memory to store the configuration data that describes the custom-designed architecture. Radiation strikes are a critical concern for SRAM-based FPGAs because they could cause an SEU, which is a change in memory state, corrupting the configuration memory. The FPGA could malfunction or operate against specifications due to configuration memory corruption. FPGAs and radiation effects are extensively described in [14]–[16].

C. Hybrid Computing

We define hybrid computing as a mix of dissimilar computing technologies to gain their collective advantages. Examples of hybrid computing are: 1) a hybrid-processor combination of dissimilar device architectures, such as a general-purpose CPU combined with an FPGA on the same

chip or on the same board; or 2) a hybrid-system combination of rad-hard devices with higher grade commercial devices to simultaneously achieve high reliability and performance.

Hybrid-processor architectures are gaining popularity in the commercial computing industry. System-on-chip (SoC) devices are the most prevalent examples of hybrid-processor architectures. These devices combine several predesigned "blocks" onto a single chip. These blocks can be embedded processors, memory blocks, interface blocks, and a variety of other components [17]. SoCs have become popular in mobile devices, embedded systems, and consumer electronics due to their low power, high performance, and ease of system integration. For this research, the SoC devices of interest are those that specifically adapt and integrate multiple computing architectures, such as a combination of CPUs, GPUs, FPGAs, and DSPs. Common examples of these architectures are Nvidia's Tegra K1, X1, and X2 (CPU+GPU) [18], Xilinx's Zynq (CPU+FPGA) [19], and TI's Keystone I and II (CPU+DSP) [20]. The main attraction of these architecture combinations is to partition applications and algorithms onto the portion of the device for which they are best suited to achieve performance gains. In [21], the authors deconstruct a common space application, hyperspectral image processing (HSI), into stages and describe how the application could be accelerated with hybrid architecture. In that paper, target detection and classification on a hyperspectral image can be divided into three stages (metric calculation, weight computation, and target classification). The metric calculation and target classification stages exhibit a large amount of fine-grained parallelism that can be best exploited by an FPGA. The middle stage (weight computation), however, is sequential in nature and best suited for a traditional CPU. A hybrid device like the Zynq can perform the entire app on a single device.

Just as hybrid-processor designs seek to exploit the benefits of different computing architectures for processing, hybrid-system design focuses on the advantage of balancing the benefits of commercial and rad-hard devices for reliability and performance. Commercial devices have the energy, cost, and performance features of the latest technology advancements; however, these devices are commonly susceptible to radiation effects in space. Commonly, commercial components do not have flight heritage or radiation-response data. Radiation-hardened and radiation-tolerant devices are relatively immune to radiation, but are more expensive, physically larger, harder to procure, and are often technology generations behind in both performance and functionality. Hybrid-system design seeks to use commercial devices, augmented by fault-tolerant computing strategies, and combined with radiation-hardened devices, to achieve the best characteristics of both devices.

D. Fault-Tolerant Computing

Space systems incorporate a variety of fault-tolerant computing techniques for reliable operation in space. Traditional fault tolerance in computing is reflected by redundancy in hardware, information, network, software, or time. Appropriate mission fault tolerance is a complex system-design challenge, because fault tolerance always introduces tradeoffs in hardware, software, performance, and cost.

Hardware redundancy is provided by incorporating additional hardware into the design, such as having three processors instead of one performing the same function (known as triple-modular redundancy). Information redundancy is exemplified by error-detection and correction coding (EDAC), error-correcting codes (ECCs), cyclic redundancy check (CRC), algorithm-based fault tolerance (ABFT), and parity checking. Network redundancy relies upon redundant network links and paths within the topology. Software redundancy is a broad category of fault tolerance, with checkpoint and recovery as well as exception handling being prominent examples. Finally, time redundancy is accomplished through repeated execution of the same program on hardware, which is primarily used to counter transient faults. The field of fault-tolerant or dependable computing is extensive and is not the focus of this discussion, therefore, more information can be found in [22].

In preparing for missions, designers should analyze their use of fault tolerance in consideration of mission requirements, since space environmental conditions vary with mission orbit. For example, certain missions may have a short duration and, therefore, parts can be selected that have much shorter lifetimes due to radiation, which would not be considered in a longer, multiyear mission. Space systems must also prioritize fault avoidance such as parts screening to avoid selecting those that are known to catastrophically fail due to radiation effects.

Due to their unique architecture, FPGA devices bring their own fault-tolerant computing strategies. Examples of these strategies include redundancy in internal logic designs and memory scrubbing, and are described in [14]–[16].

E. SmallSats and CubeSats

The rise of SmallSats can be traced to the interactions between several prominent space organizations. In 2007, the NRC, at the request of several organizations including NASA, the National Oceanic and Atmospheric Administration (NOAA), the National Environmental Satellite Data and Information Service (NESDIS), and the U.S. Geological Survey (USGS) Geography Division, conducted and published a study ("2007 decadal survey") on Earth observations from space to identify short-term needs and longer term scientific goals of importance [23]. In 2012, the NRC published a follow-up study ("midterm assessment") describing how key organizations were meeting the recommendations of the original survey [24]. From an Earth-observation perspective, there were two key findings driving SmallSat development. The first finding described that the nation's Earth-observing capabilities have begun a rapid decline as several long-running missions were ending and essential new missions were delayed, lost, or canceled. The NRC also found that NOAA's ability to meet science needs had greatly diminished due to budget

shortfalls, cost overruns, and delays. Second, the report identified the need for alternative platforms and flight formations to offer programmatic flexibility and lower the costs of meeting mission requirements and objectives. The U.S. Government Accountability Office (GAO), an office that identifies government agencies and programs that are high risk, further emphasized the critical need for new, lower cost platforms. Out of 34 total high-risk areas in 2017, the only "science and technology topic" was "Mitigating Gaps in Weather Satellite Data" describing the scenario [25] feared in the midterm assessment.

Due to these highlighted challenges, SmallSats have flourished as a technology platform. Within these constraining fiscal environments, relevant agencies, organizations, and missions are forced to achieve compelling science at lower cost and faster schedule. The underlying motivation driving SmallSats as a technology is encapsulated with the concept "do more with less." NASA and relevant organizations see value in SmallSats for a variety of reasons. SmallSats benefit from comparatively lower development costs, miniaturized electronics, and more easily accessible and affordable launch opportunities. SmallSats can also perform several key functions. First, SmallSats can be used as technology demonstrations, providing opportunities for new technology to be tested at no risk to larger programs and help to more quickly reduce the time required to advance the state of the art. SmallSats also provide unique science opportunities that cannot be achieved by a single spacecraft, such as multipoint measurements in a constellation or swarm of SmallSats. Constellations of lower cost spacecraft increase reliability and capability of a mission, since failed spacecraft can be quickly replaced. Finally, it has been suggested in [2] that CubeSats and SmallSats have the potential to mitigate data gaps, such as the gap described by GAO, allowing for sustained measurements in the short term, due to their shorter development cycles.

Michael Johnson, the NASA Chief Technologist of the Applied Engineering and Technology Directorate, described NASA interest in SmallSats [26] as follows:

> The capabilities of miniaturized systems are rapidly increasing while the resources (mass, volume, power) they require are decreasing. At the same time, NASA's fiscal environment motivates competitive projects and missions to achieve compelling science at lower cost and schedule than usual. We see small spaceflight instruments hosted by small spacecraft as a potential response to this challenge.

III. SMALLSAT COMPUTING

SmallSats are diverse platforms that can contain a wide variety of sensors, electronics, and deployables; however, a unifying common denominator that they all must include is a computing or avionics system. SmallSat computing is widely varied and can range from small microcontrollers to powerful microprocessors. This section provides an overview of SmallSat computing and its challenges, and of a new approach for future SmallSat computers, with selected examples.

A. SmallSat Technology State of the Art

In 2013, in response to the growing impact and interest in using small spacecraft, NASA's Small Spacecraft Technology Program (SSTP) commissioned a report [27] to assess key technology domains of spacecraft with mass below 180 kg. The report, however, states the bias of presenting a high emphasis on CubeSat-related technology, over SmallSats in general, due to the high market interest in CubeSats. The report describes two primary trends driving the requirements for command and data handling on small spacecraft. The first trend is the desire to introduce more complex science and technology applications, which requires high system reliability and performance. The second trend is a desire to take advantage of the low-cost, easy-to-build, accessible CubeSat development, primarily targeting hobbyists and university programs without extensive experience on spacecraft development.

In the onboard-computing section of the report, NASA observes the proliferation of microcontroller options due to the broadening number of CubeSat developers. The report compiles a list of vendor-supplied, onboard-computing solutions which, in addition to microcontrollers, contains SoCs, DSPs, and FPGAs. Table 1 extends the list in [27] for vendors of CubeSat and other SmallSat single-board computers (SBCs), along with missions upon which these devices were launched as reference. This table should not be considered an authoritative, comprehensive database of every vendor; however, it serves to provide a representation of the community. This list was extended through data supplied directly from vendors, datasheets, literary references, and personal communication. It should be noted that, since the list relies largely on publications, it will not account for changes in designs between publication and launch. In addition, several popular vendors would not disclose specific devices, due to the competition-sensitive nature of sales, and therefore are not reflected here (e.g., Blue Canyon). There were many vendors contacted, and several did not respond, so some frequently referenced designs or information is missing (e.g., Hyperion Technologies, Endurosat). Finally, no entry in the mission column does not indicate that there is no flight heritage, since some vendors could not release mission details, and many mission publications do not cite adequate detail for specific devices or SBCs to be included. Some missions cited are not SmallSats, however, this case does not preclude SmallSat missions from using a specific device.

B. SmallSat Computing Versus Traditional Spacecraft Computing

Flagship satellite missions primarily rely upon rad-hard devices to safeguard electronics from failing, since these missions are vital and expensive. Common rad-hard processors on recent missions include the Synova, Inc. Mongoose-V

Table 1 SmallSat Processors and Single-Board Computers

Device Vendor	Device	Type	SBC Vendor	SBC	Missions
Actel	ProASIC3	FPGA	Xiphos	Q7, Q6	ACES RED #1, GHGSat-D
Atmel	AT91SAM7A1	Microcontroller	GomSpace	Nanomind A712D	STRaND-1
Atmel	AT697E	Microprocessor	SwRI	SC-SPARC8 Instrument Controller	JUNO, Solar Orbiter, MMS
Atmel	AT91SAM9G20	Microcontroller	Tyvak	Intrepid	INCA
Atmel	AT32UC3C	Microcontroller	GomSpace	Nanomind A3200	GOMX-3, Dellingr
Atmel	AT91SAM9G20	Microcontroller	ISIS	OBC	QB50p1 p2, IL-02, TW-01, CN-01, BE-06, PEASSS
Atmel	ATmega329P	Microcontroller	NanoSatisfi Inc.	ArduSat Kit	ArduSat 1
Broadcom	BCM2835/6/7	SoC	RaspberryPi.org	Raspberry Pi Modules	Pi-Sat, NODeS
Cobham	UT699	Microprocessor	SEAKR	SBC	Orion VPU
Cobham Gaisler	LEON3FT	Microprocessor	SDL	MODAS Bus Interface Module	
Cobham Gaisler	GR712RC	Microprocessor	SwRI	Centaur	CYGNSS, CuSP, NASA Mission Avionics, Undisclosed
Cobham	UT699	Microprocessor	SwRI	FT Spacecraft/Instrument Controller	JUNO, FERMI, Kepler, DoD Mission
Freescale	P2020	Microprocessor	Space Micro	Proton400k	ORS-1
Microchip	PIC24FJ256GA110	Microcontroller	Pumpkin	PSPM D	MiRaTA, MicroMAS-1, FIREBIRD-I
Microchip	PIC24F256GB210	Microcontroller	Pumpkin	PSPM E	
Microchip	PIC24FJ256GA110	Microcontroller	Pumpkin	PPM D1	Caerus/Mayflower, DICE-1, DICE-2, Aeneas
Microchip	dsPIC33FJ256GP710	Microcontroller	Pumpkin	PPM D2	CINEMA
Microchip	ATmegaS128	Microcontroller	Undisclosed	Undisclosed	Undisclosed
Microsemi	SmartFusion 2	SoC	Clyde Space	OBC	
Microsemi	SmartFusion 2	SoC	NSF SHREC ctr.	µCSP	STP-H6/SSIVP
Nvidia	Tegra	SoC	Innoflight	TFLOP	Undisclosed
NXP	MPC8548E	Microprocessor	Aitech	SP0	MUSES
NXP	MPC7457	Microprocessor	SEAKR	G4	Artemis TacSat 3
NXP	MPC8548E	Microprocessor	SwRI	High-Performance SBC	Undisclosed
Silicon Labs	EFM32GG280F1024	Microcontroller	CubeSpace	CubeComputer	
Silicon Labs	C8051F120	Microcontroller	Pumpkin	PSPM B	
Silicon Labs	C8051F120	Microcontroller	Pumpkin	PPM B1	QbX1, QbX2
Sitara	AM3359AZCZ100	Microprocessor	BeagleBoard.org	BeagleBone Black (Rev C)	RADSat, ANDESITE, TRYAD
Texas Instruments	Sitara AM3703	Microprocessor	Gumstix	Overo EarthSTORM	IPEX
Texas Instruments	OMAP3530	Microprocessor	Gumstix	Overo Water	DM7
Texas Instruments	MSP430F1612	Microcontroller	Pumpkin	PPM A1	CSSWE
Texas Instruments	MSP430F1611	Microcontroller	Pumpkin	PPM A2	
Texas Instruments	MSP4302618	Microcontroller	Pumpkin	PPM A3	
Texas Instruments	MSP430F149/169/1611/1612	Microcontroller	Pumpkin	FM430	Delfi-C3, HawkSat-1, ITU-pSAT1, AIS Pathfinder 2, GOLIAT, e-st@r,Libertad-1
Texas Instruments	TI320C6713DSP	DSP	SDL	MODAS CPU Module	
Texas Instruments	TI 320C6XXXDSP	DSP	Space Micro	Proton200k	MDA MISTI, Goodrich, QuickReach
Xilinx	Zynq 7030	SoC	GomSpace	NanoMind Z7000	GOMX-3
Xilinx	Zynq 7020	SoC	Innoflight	CFC-300	Undisclosed
Xilinx	Zynq 7045	SoC	Innoflight	INNOF6TP	Undisclosed
Xilinx	Ultrascale+	SoC	Innoflight	CHAMPS Flight Computer	Undisclosed
Xilinx	Artix-7	FPGA	MSU	N/A	RadSat
Xilinx	Zynq 7045	FPGA	Raytheon	S3OP	
Xilinx	Virtex-7	FPGA	Space Micro	Proton300k	ORS-1, Undisclosed, TESS
Xilinx	Zynq 7020	SoC	NSF SHREC ctr./ Space Micro	CSPv1	STP-H5, SkyFIRE, CeREs, Luna-H
Xilinx	XCV800	FPGA	Surrey Space Center	SSTRL OBC	
Xilinx	Virtex-4	FPGA	Tohoku University	MPU	RAIKO
Xilinx	Zynq 7020	SoC	Xiphos	Q7	ACES RED #1, GHGSat-D
Xilinx	Spartan-6	FPGA	Xiphos	Q6	OSTEO-4
Xilinx	Virtex II-Pro	SoC	Xiphos	Q5	Genesis-1, Genesis-2
Xilinx	UltraScale+	SoC	Innoflight	TFLOP	Undisclosed
Xilinx	V5-QV	FPGA	NASA GSFC	SpaceCube 2.0	RRM3, Restore-L, NEODaC, RAVEN, XCOM

(New Horizons), BAE RAD6000 (DSCOVR), BAE RAD750 (GPM, JWST, Curiosity Rover), and Cobham Gaisler LEON-3FT (Hayabusa2), which have extensive flight heritage. The RAD750 is emphasized as a state-of-the-art flight device, comes in standardized CompactPCI (cPCI) 3U or 6U sizes [28], and consumes a total power of 5 W [29]. Notably, these devices are based on much older designs than current commercial devices due to the considerable financial and schedule investment required to develop new rad-hard products. Using the device-metrics approach described in [29], Fig. 2 shows the performance normalized by power consumption of selected devices of interest: microcontrollers (blue), rad-hard (red), microprocessors (black), FPGAs (green), and SoCs (Purple). This figure illustrates several key outcomes. First, as expected, standard microcontrollers have negligible performance compared to other device categories. The chart also highlights the poor performance of rad-hard processors compared to commercial devices. Finally, the figure displays the vast performance advantages to be gained with SoCs. Due to the difficulty of obtaining device information, several assumptions regarding device operations had to be made for Fig. 2. An example of an assumption made is the number of operations per cycle for 8- and 16-b integers if not explicitly stated. Additionally, the BCM2835 was scaled by board power instead of the expected device power (information not available). Additional performance analysis on the capability of other rad-hard devices is presented in [29]. Another study conducted in 2012 by Ramon chips [30] compares both rad-hard devices and commercial devices augmented with fault-tolerant strategies.

Due to the cost of rad-hard devices, mission budget is the motivating consideration between SmallSat computing and traditional spacecraft computing. Fig. 3 displays the cost of several commercial SBCs, where prices were easily identifiable. It should be noted that, for a large number of vendors, SBC prices require a quote or nondisclosure agreement and therefore are not included in this figure. This chart

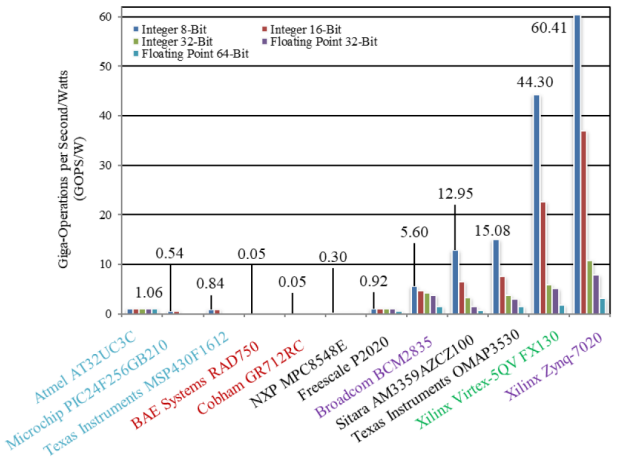

Fig. 2. ***Performance scaled by power comparison of onboard processors.***

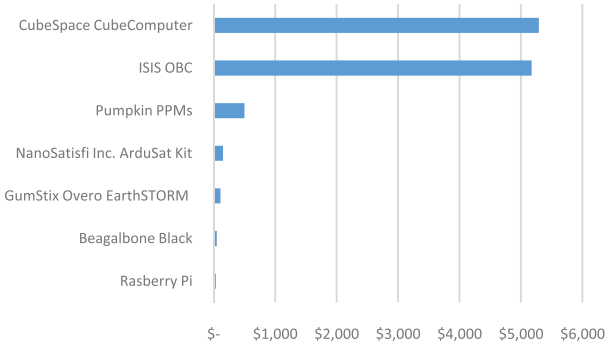

Fig. 3. ***Costs of commercially available SBCs.***

emphasizes the difference between these commercially available devices and rad-hard boards that can cost orders of magnitude more than some commercial options.

SmallSat missions may lack the budget to include all rad-hard electronics; however, they are excellent platforms for new-technology demonstration. The primary benefit for SmallSats from a computing perspective stems from the reuse of devices on SmallSats in larger mission satellites. Reference [27] cites CompactPCI is cited as a common SmallSat bus, and shows that common SmallSat power solutions can also support the power profiles of some rad-hard devices. A use case is demonstrated in [31], with engineers from the Information Sciences Institute seeking to fly an experimental, multicore, rad-hard processor to be validated on the small NovaWorks platform.

Perhaps the most overt demonstration of using any commercial electronics was observed in a precedent set by NASA Ames Research Center and the PhoneSat program. In these experiments, NASA demonstrated that they could fly common cellphones (Nexus One, Nexus S smartphones) and basic electronics in space for a short period [32].

C. Challenges to SmallSat Computing

The challenges of SmallSat (including CubeSat) computing are largely related to the challenges faced by SmallSats as a development platform. SmallSats, compared to large satellites, have reduced size, weight, power, cost, and volume. These requirements also restrict the capabilities of a single-board computer. General CubeSat trends and failures are considered by Swartout's presentations analyzing the St. Louis University CubeSat database [33]. General SmallSat challenges have also been addressed by NASA in the Small Spacecraft Reliability Initiative [34].

The primary challenge facing SmallSat computing resides in the use of commercial processors. Since commercial processors are not hardened for radiation, they are affected by radiation effects as previously described. In addition, modern SoCs and FPGAs are complex devices that contain additional IP blocks such as on-chip memory, clock management, and interface controllers. These different components all require separate radiation tests to determine

each individual component's error modes and upset rates. This realization further complicates the design process, as radiation testing is both time consuming to plan effective tests and conduct actual testing. Last, radiation testing is very expensive, which prohibits many organizations from testing the devices they fly.

Commercial devices are constantly pushing the bounds of new technology and interact with radiation in different ways, occasionally exhibiting new effects never before observed on other devices. In [35], Lee *et al.* describe an unconventional single-event latch-up, also called "micro latchup," that was discovered in new FPGA technology used for flight missions.

University programs and hobbyists rely on commercial off-the-shelf CubeSat kits, both for convenience and simplicity of development. Steven Guertin at NASA Jet Propulsion Lab (JPL) has been conducting studies on common CubeSat microcontrollers and microprocessors found in CubeSat kits, starting with his initial report in 2014 [36], with follow-up reports each year at NEPP. His testing reveals that, while relatively resilient to TID for low Earth orbit (LEO), most of these CubeSat kit devices show significant problems caused by latchup. These results do not guarantee that a device will fail; however, they highlight that during a low-probability event in LEO, the device may suffer from significant issues. The Air Force Research Laboratory has also conducted independent testing on common commercial kits in [37].

The last challenge, highlighted by NASA Goddard's presentation on [38], is that certain tasks such as flight software, communications, ground systems, and attitude control system, fundamentally require the same functions as larger spacecraft with comparable analysis and testing. Their mission made compromises to sensor data acquisition to perform all the desired flight-software processing onboard with the selected microcontroller.

D. Better Computing With Hybrid Approach

Next-generation spacecraft missions seek to accomplish even more significant science and defense objectives with SmallSats. New missions are proposed for more-challenging radiation environments than LEO, including Lunar, Mars, and deep space. To accomplish these objectives, computing will have to achieve a sufficiently high level of both performance and radiation reliability.

Rudolph *et al.* [39] propose a multifaceted, hybrid-design methodology to achieve the benefits of both commercial and rad-hard designs. This approach proposes a hybrid-system architecture, where commercial technology is featured for high performance and energy efficiency, while the device is supported and managed by rad-hard components for increased reliability. Additionally, the reliability is bolstered by fault-tolerant computing strategies applied atop the commercial device. This hybrid approach also describes use of a hybrid device (e.g., CPU+FPGA SoC) as the featured commercial processor to maximize performance by optimizing algorithms based upon architecture needs.

E. Single-Board Computer (SBC) Examples

This section provides an overview of some unique, hybrid-architecture designs for SmallSat computing. There are many potential vendor designs that could also be described here. However, many vendors do not provide readily available information and scholarly publications elaborating design decisions in greater detail.

Computer: CSPv1

Design: NSF SHREC Center (Vendor: Space Micro)

Missions: STP-H5/ISEM-CSP, STP-H6/SSIVP, Lockheed Martin Skyfire CubeSat, NASA Goddard CeREs CubeSat

Classification: hybrid processor, hybrid system

Reference: [39], [40]

The CHREC Space Processor v1 (CSPv1) design demonstrates both hybrid-processor and hybrid-system design. The core hybrid-processing technology featured is the Xilinx Zynq-7020 SoC combining fixed (dual ARM Cortex-A9/NEON cores) and reconfigurable (Artix-7 FPGA fabric) logic. The intended flight architecture focuses on using commercial components (Zynq with DDR memory) for performance, while using rad-hard components (supporting power management, reset control and circuitry, and nonvolatile memory) for reliability. The CSPv1 also uniquely enables the cost and reliability of the design to be varied by providing both commercial and rad-hard footprints for some components. The CSPv1 fits a 1U CubeSat form factor, with a maximum power of 2.86 W. This design is provided in Fig. 4. The Zynq SoC supplies orders of magnitude performance increases compared to the RAD750. Since its initial launch in February 2017 on STP-H5, the CSPv1 has proven to be a reliable design, with no significant failures in its operations to date.

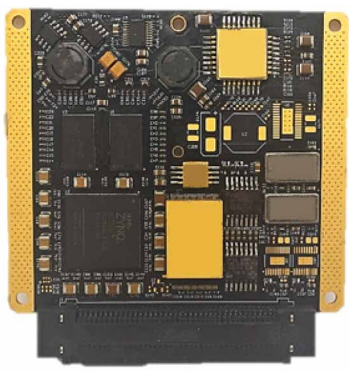

Fig. 4. ***CSPv1 Rev. B. Flight Computer.***

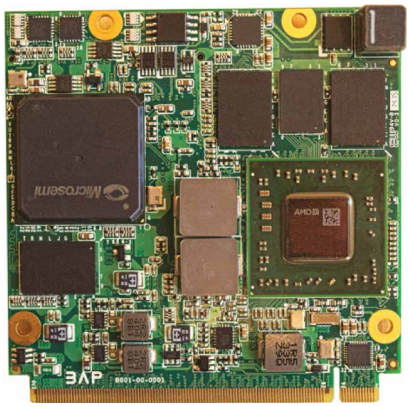

Fig. 5. *Unibap e2000 flight computer as seen in [42].*

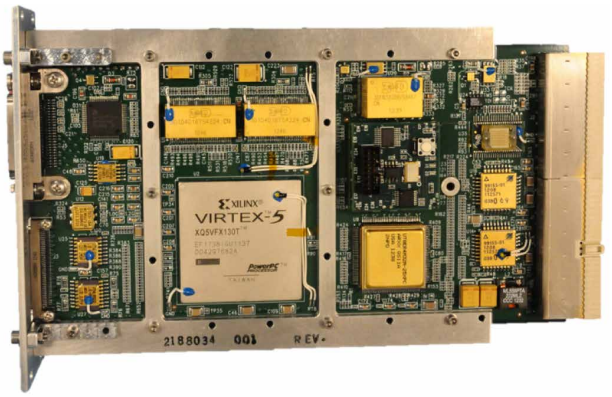

Fig. 6. *NASA GSFC SpaceCube 2.0 flight computer (courtesy: NASA GSFC).*

Computer: e2000

Design: Unibap

Missions: Nusat 1 and NuSat 2 with more expected with Satellogic Aleph-1 Constellation

Classification: hybrid processor

Reference: [41], [42]

The e2000 is a heterogeneous computer targeting onboard, intelligent data processing and autonomy, developed by the Swedish company Unibap. This design relies on screened and derated commercial components and is unique because it features two hybrid processors: the AMD SoC FT3 "eKabini" and the Microsemi SmartFusion2 SoC. The AMD G-series SoC FT3 "eKabini" GX415GA features quad-core "Jaguar" x86 cores and an AMD Radeon HD 8201. The Microsemi SmartFusion2 SoC features an ARM Cortex-M3 processor and a flash-based FPGA fabric. The e2000 design conforms to the computer-on-module standard Qseven (70 mm × 70 mm). Despite having a high thermal-design power, with an OpenCV image-processing load the engineering design performed nominally at 6 W. The e2000 design is pictured in Fig. 5.

Computer: SpaceCube 2.0

Design: NASA Goddard Space Flight Center (GSFC)

Missions: STP-H4/ISE2.0, STP-H5/Raven, STP-H6/XCOM, RRM3, Restore-L, NEODaC

Classification: hybrid processor, hybrid system

Reference: [43]

SpaceCube 2.0 is the latest in the family of FPGA onboard-processing systems from NASA GSFC. There are two Virtex-5 FPGAs linked by a high-speed interconnect. The featured hybrid processor is a Xilinx Virtex-5 XC5VFX130T, which includes two PowerPC 440 RISC hard-core CPU blocks and a robust FPGA fabric. SpaceCube has a unique hybrid-system architecture, as the various peripherals and power circuitry are space-grade and rad-hard, and it also features a radiation-tolerant Aeroflex UT6325 that is responsible for monitoring, configuring, and scrubbing the Xilinx FPGAs. The design for the Virtex-5 is pin-compatible with the space-grade version of the device, the Xilinx V5-QV. The SpaceCube 2.0 processing card is based on an extended version of the 3U cPCI form factor at 190 mm × 100 mm, with a maximum power of 10 W. SpaceCube 2.0 is pictured in Fig. 6.

Computer: LANL SBC

Design: Los Alamos National Laboratory (LANL)

Missions: undisclosed DoD Satellite for 2019

Classification: hybrid system

Reference: [44]

The LANL SBC was developed by the Intelligence and Space Research Division at Los Alamos National Laboratory with the goal of providing a complete space-grade, rad-hard payload processor for medium Earth orbit (MEO) and geostationary Earth orbit (GEO) applications. The driving development was to achieve better performance at lower cost than the commonly used BAE RAD750. The design consists solely of flight-grade (QML V and Class S) components. The LANL SBC provides a hybrid-system design including the Cobham Gaisler GR712RC, dual-core LEON3 processor, and the SEU-immune Microsemi RTG4 FPGA fabric. The LANL SBC leverages the MicroTCA standard, which is smaller than the standard 6U cPCI. Nominally, the SBC consumes about 6 W of power. This board is pictured in Fig. 7.

Additional hybrid designs were identified from literature survey, however, no literary references on design choices were available. SRI Inc. features an Nvidia Tegra K1 (quad-core ARM Cortex-A15 MPCore R3+ low power companion core and "Kepler" GK20A GPU) with a Xilinx Kintex-7 FPGA. The Q7 board by Xiphos features

Fig. 7. ***LANL SBC as seen in [44].***

a ProASIC3 and Zynq 7020. Finally, the Hybrid OBC by Moscow Institute of Physics and Technology features a ProASIC3 and Virtex-6 [45].

IV. ROADMAP

Advances in SmallSat computing bring drastic benefits to developments in general space computing, because popular SBCs used on large, flagship missions can also conform to fit in a SmallSat and, conversely, SBCs used in SmallSats can also be used for larger spacecraft and missions. SmallSat technology-demonstration missions for computing are therefore extremely useful because they demonstrate device viability to missions of all sizes. This section describes predictions for the future directions of SmallSat computing. Section IV-A describes the need for better computing in next-generation systems with SmallSat Constellations. Sections IV-B and IV-C describe potential devices that will help small spacecraft accomplish future goals.

A. Concepts for Constellations of SmallSats

For the past decade, there have been considerations and discussions on replacing large, monolithic spacecraft missions with smaller, fractionated spacecraft. Originally described in [46], the fractionated-spacecraft concept focuses on splitting up the capability of one large spacecraft into multiple smaller spacecraft, ultimately providing equivalent functionality. This paper describes several principal concepts including architectural flexibility (deploying additional nodes as demand scales), risk reduction (by avoiding a single launch failure which can end a mission or replacing nodes should they fail), engineering-complexity reduction (simpler nodes with reduced requirements), and reduced costs (launch-weight savings, secondary payload launches, market growth and competition). This concept was embodied in the Defense Advanced Research Projects Agency (DARPA) project System F6 (Future, Fast, Flexible, Fractionated, Free-Flying spacecraft). While the flight experiment was ultimately unsuccessful, lessons learned have been key drivers for future mission proposals. The program included several overlapping "technology pillars," significantly distributed computing, distributed payload operations, and cluster operations, all being major computing challenges [47].

This concept was also emphasized by the Air Force Space Command (AFSC) in a white paper from 2013 entitled "Resiliency and Disaggregated Space Architectures," that primarily focused on mission survivability and affordable capabilities. From the AFSC perspective, more satellites increase the number and diversity of targets complicating an adversary's calculations and actions to disable a system [48]. In 2014, the GAO published a report citing that additional knowledge would be needed before supporting further disaggregation of large satellites. GAO noted that the DoD needs to expand demonstration efforts to examine the operational feasibility of disaggregation. Moving forward, SmallSats are a low-cost method of proving fractionated designs and concepts [49].

The NRC notes other mission concepts beyond deconstructing a single spacecraft for new science opportunities. In [2], the NRC describes a mission concept in the decadal survey, a Geospace Dynamics Constellation, which requires identical satellites providing critical measurements in different locations. This mission requires essentially simultaneous, multipoint measurements, which is a science goal that cannot be achieved with a single spacecraft and is uniquely suited to small spacecraft. Also, noted in the report is the challenge of additional computational requirements and capabilities demanded by flight software for managing and coordinating the large number of these spacecraft. Finally, another common factor across all space missions is the operational cost, including ground stations and personnel. Future missions will need to emphasize automation because, for a constellation to be fiscally viable, it should not scale with operational costs (i.e., the number of ground operators should not need to grow proportionally to the number of satellites in the constellation). Deep learning and artificial intelligence could be critical for space applications, allowing a small operations team to control an entire constellation. However, the viability of these autonomous applications in terrestrial applications relies on large, distributed systems with GPUs, which is infeasible on a space system without improved next-generation computing devices and optimized platform applications.

B. High-Performance Spaceflight Computing Project

In 2012, the NASA Game Changing Development Program (GCDP) commissioned a High-Performance Spaceflight Computing (HPSC) formation activity to determine a new general-purpose computing architecture for next-generation NASA missions to replace the BAE

RAD750. It was cited that space-based computing has not kept up with the requirements of current and future NASA missions. Common interest between the AFRL and the NASA HPSC activity developed into an agency-level partnership called the Next-Generation Space Processor (NGSP). A series of workshops were held between scientists, engineers, and mission designers to identify use-case applications to determine what would be needed. Use-case examples, applicable applications, and findings of the research effort are described in [50].

As previously described due to cost limitations, rad-hard computers will not see widespread use in many SmallSat programs. However, rad-hard device requirements excluding cost (e.g., form factor, power) do not prohibit its use on SmallSat platforms. It is likely that the first prototypes for HPSC will be tested on SmallSats before being included on more expensive missions and programs.

C. Compelling Devices

This section describes both popular and upcoming devices to be considered for SmallSat computing, categorized by device type. This section does not discuss microcontrollers, since they lack adequate processing capabilities for next-generation science and defense missions. Microcontrollers, however, will continue to be prevalent in the CubeSat market, since they are well suited as an educational tool. It should also be noted that while the following devices are strong candidates for study, the NASA Ames PhoneSat program proves that, with SmallSats, there is opportunity to fly nearly any device that will meet physical restrictions. Radiation considerations for many of the following devices can be found in the NEPP technology roadmap in [51].

1) FPGAs: FPGAs provide large utility to any mission, especially for payload interfacing and availability of softcore processors. The Xilinx Virtex, Kintex, and Artix 7-series family will all continue to be well used. There have also been studies on the Kintex UltraScale. The Microsemi RTG4 may gain popularity with flight programs since Microsemi is seeking QML Class Q and Class V qualifications, however, many small missions may be unable to afford them. A more likely candidate for study may be the new Microsemi PolarFire FPGA.

2) CPUs: The commercial market is continuously developing new devices that could also be featured on small spacecraft. Example technologies include new 14-nm FinFET and smaller devices under production by Intel, AMD, and Samsung. For rad-hard devices, Cobham will have flight models of the GR740 Quad-Core LEON4 SPARC V8 processor. Expected soon is the new BAE Systems RAD5545 multicore processor.

3) GPUs: While GPUs have not been traditionally considered for space missions, due to their high power-profile requirements, they are rapidly making an appearance as part of SoC systems. NEPP has plans to test 14-nm GPUs from Nvidia and AMD, along with the 14-nm Nvidia Tesla.

4) System-on-Chip (SoC) Devices: As highlighted in Table 1, common SoC devices for space include the Xilinx Zynq-7000s, Microsemi SmartFusion2, and Xilinx Virtex-5. As a natural evolution from the Zynq-7000 family, new boards will likely focus on the Xilinx UltraScale+ MPSoC. This family is much more capable than its precursor, including quad ARM Cortex-A53 cores, dual Cortex-R5 real-time cores, and a large 16-nm FinFET+ programmable-logic fabric. Several companies and vendors have announced plans for this device on future space designs.

Intel/Altera is a common commercial-FPGA vendor that has not had a strong historical presence in space computing. New SoCs used in SmallSats may include the Arria-10 SoC, which features a dual-core ARM Cortex-A9 MPCore and FPGA fabric, and the Stratix-10, featuring quad ARM Cortex-A53s cores and a potent FPGA fabric.

Another key interest for the space community will be the Nvidia Tegra K1, X1, and X2 hybrid GPUs. These devices are reportedly to be used by spacecraft vendors on new designs. Additionally, the science community is studying the potential of these embedded systems for Earth observations [52].

5) Neuromorphic Devices: Neuromorphic computational devices are new to the general terrestrial computing scene; however, researchers and companies are already investigating these architectures for space processing. The IBM TrueNorth device has been used by SRI for studies in optical and SAR classification [53]. NASA also has tentative plans on its technology roadmap to test the KnuEdge Hermosa and Hydra.

V. CONCLUSION

SmallSats are rapidly becoming more commercially viable and are redefining the space industry. As more launch opportunities develop, more industry, government, and university programs have begun to participate in small-spacecraft missions. Organizations such as Planet Labs, Inc., Doves constellation, ESA's QB50 project, and University of Michigan with Southwest Research Institute's Cyclone Global Navigation Satellite System (CYGNSS) are proving the commercial value and significant science capability of swarms of SmallSats. Prominent space organizations have identified future science and defense objectives that can be accomplished with small spacecraft. Additionally, these organizations have proposed specific mission concepts only viable with constellations of SmallSats.

Onboard computing is a crucial aspect of SmallSat design, because high-performance computers are needed

to meet the algorithmic and computational challenges proposed by new missions. Common onboard-computing solutions for missions, however, are dominated by commercial CubeSat kits, which typically feature limited microcontrollers as the primary device. Additionally, many SmallSat programs create all commercial solutions that are susceptible to radiation. Radiation-hardened processors help avoid the hazards of radiation effects, but their performance may lag behind requirements of future missions and they can be prohibitively expensive. To both meet critical reliability and performance requirements for future missions, designers are turning to a new computing approach focusing on two themes: reconfigurable computing and hybrid computing. This paper has highlighted concepts, with examples of current single-board computers that feature combinations of these principles and technologies, to achieve greater performance and versatility within the constraints of a SmallSat system. ■

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REFERENCES

[1] *The Role of Small Satellites in NASA and NOAA Earth Observation Programs*, National Academy Press, Washington, DC, USA, 2000. [Online]. Available: https://www.nap.edu/catalog/9819/the-role-of-small-satellites-in-nasa-and-noaa-earth-observation-programs

[2] *Achieving Science With CubeSats: Thinking Inside the Box*, National Academy Press, Washington, DC, USA, 2000. [Online]. Available: https://www.nap.edu/catalog/23503/achieving-science-with-cubesats-thinking-inside-the-box

[3] B. Doncaster, C. Williams, and J. Shulman (2017). *Nano/Microsatellite Market Forecast*. [Online]. Available: http://spaceworksforecast.com/docs/SpaceWorks_Nano_Microsatellite_Market_Forecast_2017.pdf

[4] *NASA Technology Roadmaps*, NASA, Washington, DC, USA, 2015. [Online]. Available: https://www.nasa.gov/offices/oct/home/roadmaps/index.html

[5] *NASA Space Technology Roadmaps and Priorities Revisited*, National Academy Press, Washington, DC, USA, 2000. [Online]. Available: https://www.nap.edu/catalog/23582/nasa-space-technology-roadmaps-and-priorities-revisited

[6] J. Hyten, "Small satellite 2015 keynote speech," in *Proc. 29th Annu. AIAA/USU Conf. Small Satellites*, Logan, UT, USA, Aug. 2015. [Online]. Available: http://www.afspc.af.mil/About-Us/Leadership-Speeches/Speeches/Display/Article/731705/small-satellite-2015-keynote-speech/

[7] J. R. Schwank, M. R. Shaneyfelt, and P. E. Dodd, "Radiation hard-ness assurance testing of microelectronic devices and integrated circuits: Radiation environments, physical mechanisms, and foundations for hardness assurance," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 2074–2100, Jun. 2013.

[8] L. D. Edmonds, C. E. Barnes, and L. Z. Scheick, "An introduction to space radiation effects on microelectronics," NASA, Washington, DC, USA, Tech. Rep. JPL00-06, May 2000. [Online]. Available: https://snebulos.mit.edu/projects/reference/NASA-Generic/JPL-00-06.pdf

[9] F. W. Sexton, "Destructive single-event effects in semiconductor devices and ICs," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 603–621, Jun. 2003.

[10] R. H. Maurer, M. E. Fraeman, M. N. Martin, and D. R. Roth, "Harsh environments: Space radiation environment, effects, and mitigation," in *Johns Hopkins APL Tech. Dig.*, 2008, vol. 28. no. 1, p. 17. [Online]. Available: http://techdigest.jhuapl.edu/TD/td2801/Maurer.pdf

[11] K. A. LaBel and M. J. Sampson, "The NASA electronic parts and packaging program," in *NASA Electronics Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW)*. Greenbelt, MD, USA: NASA Goddard Space Flight Center, Jun. 2016.

[12] K. A. LaBel, A. H. Johnston, J. L. Barth, R. A. Reed, and C. E. Barnes, "Emerging radiation hardness assurance (RHA) issues: A NASA approach for space flight programs," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2727–2736, Dec. 1998.

[13] K. A. LaBel, "NEPP radiation effects 101," NASA, Greenbelt, MD, USA, Tech. Rep., Apr. 2004.

[14] M. Berg and K. LaBel, "Introduction to FPGA devices and the challenges for critical application: A user's perspective," in *Proc. Hardened Electron. Radiat. Technol. (HEART)*, Chantilly, VA, USA, Apr. 2015.

[15] M. Wirthlin, "High-reliability FPGA-based systems: Space, high-energy physics, and beyond," *Proc. IEEE*, vol. 103, no. 3, pp. 379–389, Mar. 2015.

[16] A. Jacobs, G. Cieslewski, A. George, A. Gordon-Ross, and H. Lam, "Reconfigurable fault tolerance: A comprehensive framework for reliable and adaptive FPGA-based space computing," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 5, no. 4, pp. 1–30, Dec. 2012.

[17] R. Saleh *et al.*, "System-on-chip: Reuse and integration," *Proc. IEEE*, vol. 94, no. 6, pp. 1050–1069, Jun. 2006.

[18] *NVIDIA Tegra K1 A New Era in Mobile Computing*, Nvidia Corp., Santa Clara, CA, USA, Tech. Rep., Jan. 2014.

[19] "Zynq-7000 all programmable SoC data sheet: Overview," Xilinx, San Jose, CA, USA, Tech. Rep. DS190, Jun. 2017.

[20] "66AK2Hxx multicore DSP+ARM KeyStone II system-on-chip (SoC)," Texas Instruments, Sherman, TX, USA, Tech. Rep. SPRS866F, Jun. 2017.

[21] A. Jacobs, C. Conger, and A. D. George, "Multiparadigm space processing for hyperspectral imaging," in *Proc. IEEE Aerosp. Conf.*, Big Sky, MT, USA, Mar. 2008.

[22] I. Koren, C. M. Krishna, *Fault Tolerant Systems*. San Francisco, CA, USA: Morgan Kaufman, 2007.

[23] *Earth Science and Applications from Space: National Imperatives for the Next Decade and Beyond*, National Academy Press, Washington, DC, USA, 2007. [Online]. Available: https://www.nap.edu/catalog/11820/earth-science-and-applications-from-space-national-imperatives-for-the

[24] *Earth Science and Applications from Space: A Midterm Assessment of NASA's Implementation of the Decadal Survey*, National Academy Press, Washington, DC, USA, 2012. [Online]. Available: https://www.nap.edu/catalog/13405/earth-science-and-applications-from-space-a-midterm-assessment-of

[25] *U.S. Government Accountability Office*, Washington, DC, USA. (2017). *2017 High-Risk Report*. [Online]. Available: http://www.gao.gov/assets/690/682765.pdf

[26] N. Cheeks, "CabeSat/SmallSat," *NASA Goddard Tech. Transf. News*, vol. 12, no. 3, pp. 7–15, 2014. [Online]. Available: https://partnerships.gsfc.nasa.gov/wp-content/uploads/TechTransfer-Summer2014.pdf

[27] "Small spacecraft technology state of the art," NASA, Washington, DC, USA, Tech. Rep. NASA/TP-2015-216648/REV, Jul. 2017. [Online]. Available: https://sst-soa.arc.nasa.gov

[28] "RAD750 family of radiation-hardened products," BAE Syst., Farnborough, U.K., Tech. Rep. CS-16-F80.

[29] T. M. Lovelly and A. D. George, "Comparative analysis of present and future space-grade processors with device metrics," *AIAA J. Aerosp. Inf. Syst.*, vol. 14, no. 3, pp. 184–197, Mar. 2017.

[30] R. Ginosar, "Survey of processors for space," in *Proc. DASIA*, Dubrovnik, Croatia, May 2012.

[31] C. Rodgers, D. Barnhart, and S. Crago, "Maestro flight experiment: A 49-core radiation hardened processor in space," in *Proc. IEEE Aerosp. Conf.*, Big Sky, MT, USA, Mar. 2016.

[32] J. Cockrell, B. Yost, and A. Petro, "PhoneSat—The smartphone nanosatellite," Tech. Rep. NASA FS-2013-04-11-ARC, Jul. 2013. [Online]. Available: https://ntrs.nasa.gov/search.jsp?R=20140005553

[33] M. A. Swartwout, "CubeSats and mission success: 2017 update," presented at the Electron. Technol. Workshop, NASA Electron. Parts Packag. Program (NEPP) Electron. Technol. Workshop (ETW), Greenbelt, MD, USA, Jun. 2017.

[34] M. Johnson *et al.*, "Increasing small satellite reliability—A public-private initiative," in *Proc. Annu. AIAA/USU Conf. Small Satellites, Big Picture Session*, Logan, UT, USA, Aug. 2017.

[35] D. Lee, M. Wirthlin, G. Swift, and A. Le, "Single-event characterization of the 28 nm Xilinx Kintex-7 field-programmable gate array under heavy ion irradiation," in *Proc. Radiation Effects Data Workshop (REDW)*, Jul. 2014.

[36] S. Guertin, "Candidate CubeSat Processors," in *Proc. NASA Electron. Parts Packag. (NEPP) Program EEE Parts Small Missions Workshop*, Greenbelt, MD, USA, Sep. 2014.

[37] K. Avery *et al.*, "Total dose test results for CubeSat electronics," in *Proc. Radiation Effects Data Workshop (REDW)*, Jul. 2011.

[38] C. Clagett *et al.*, "Dellingr: NASA goddard space flight center's first 6U spacecraft," in *Proc. Annu. AIAA/USU Conf. Small Satellites*, Logan, UT, USA, Aug. 2017.

[39] D. Rudolph *et al.*, "CSP: A multifaceted hybrid system for space computing," *Proc. 28th Annu. AIAA/USU Conf. Small Satellites*, Logan, UT, USA, Aug. 2014.

[40] C. Wilson *et al.*, "CSP hybrid space computing for STP-H5/ISEM on ISS," in *Proc. 29th Annu. AIAA/USU Conf. Small Satellites*, Logan, UT, USA, Aug. 2015.

[41] F. Bruhn, K. Brunberg, J. Hines, L. Asplund, and M. Norgren, "Introducing radiation tolerant heterogeneous computers for small satellites," in *Proc. IEEE Aerosp. Conf.*, Big Sky, MT, USA, Mar. 2015, pp. 1–10.

[42] F. Bruhn and I. Troxel, "GPU for small satellites and AI applications," in *Proc. Fault-Tolerant Spaceborne Comput. Employing New Technol. Workshop*, Albuquerque, NM, USA, May/Jun. 2017.

[43] D. Petrick *et al.*, "SpaceCube v2.0 space flight hybrid reconfigurable data processing system," in *Proc. IEEE Aerosp. Conf.*, Big Sky, MT, USA, Mar. 2014.

[44] R. Merl and P. Graham, "A low-cost, radiation-hardened single-board computer for command and data handling," in *Proc. IEEE Aerosp. Conf.*, Big Sky, MT, USA, Mar. 2016.

[45] A. Zlobin, S. Podshivalov, T. Kondranin, and S. Negodyaev, "Low-cost reliable onboard computer for Small Satellites," in *Proc. 29th Annu. AIAA/USU Conf. Small Satellites*, Logan, UT, USA, Aug. 2015.

[46] O. Brown and P. Eremenko, "The value proposition for fractionated space architectures," in *Proc. AIAA Space Conf.*, San Jose, CA, USA, Sep. 2006.

[47] O. Brown, "*System F6 program overview*," NASA Colloquium, Feb. 2007.

[48] *Resiliency and Disaggregated Space Architectures*. Air Force Space Command, 2013.

[49] *U.S. Government Accountability Office*, Washington, DC, USA.(2014). *Additional Knowledge Would Better Support Decisions About Disaggregating Large Satellites*. [Online]. Available: http://www.gao.gov/assets/670/666716.pdf

[50] R. Doyle, W. Powell, G. Mounce, M. Goforth, S. Horan, and M. Lowry, "High performance spaceflight computing (HPSC) next-generation space processor (NGSP) a joint investment of NASA and AFRL," in *Proc. Int. Symp. Artif. Intell., Robot. Autom. Space (i-SAIRAS)*, Montreal, Canada, Jun. 2014.

[51] K. LaBel, "NEPP technology planning," in *NASA Electronics Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW)*, NASA, Greenbelt, MD, USA, Jun. 26-29, 2017.

[52] L. Riha, J. Le Moigne, and T. El-Ghazawi, "Optimization of selected remote sensing algorithms for many-core architectures," *IEEE J. Sel. Topics Appl. Earth Observ. Remote Sens.*, vol. 9, no. 12, pp. 5576–5587, Dec. 2016.

[53] J. Grabowski, "Neuromorphic computing for classification in optical and SAR data with the IBM TrueNorth and FPGAs," in *Proc. Fault-Tolerant Spaceborne Comput. Employing New Technol. Workshop*, Albuquerque, NM, USA, May/Jun. 2017.

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